SELECTIVE AREA EPITAXY OF III-V NANOWIRES: TOWARD NANOWIRE-ON-SILICON TANDEM SOLAR CELLS

BY

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DISSERTATION

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ABSTRACT

Nanowires grown via the selective area epitaxy technique (SAE-NWs) are of great research interest for use in next-generation electronic and electro-optic devices. As compared to other nanowire growth techniques commonly studied, SAE-NW is a highly controllable process due to the use of a lithographically defined growth mask, and the lack of need for a catalytic seed particle results in impurity-free material with nearly atomically flat sidewalls formed on low index crystal facets. In this thesis, the SAE-NW growth technique is examined and progress in the field is reviewed. A study of the geometric evolution of SAE-NWs during growth is presented, followed by results of efforts to work towards fabrication of a tunnel diode for use in a nanowire-on-silicon solar cell. Finally, future directions for the continued study of SAE-NWs are outlined.

To my parents

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CHAPTER 1

INTRODUCTION

1.1 The Ultimate Disruptive Technology

Over the past century, the world has experienced an unprecedented period of technical advancement. The constant scientific discovery has fueled engineering efforts to develop new technologies and find applications for them. Of all the many and varied fields of science and engineering, the development of the semiconductor industry over the last several decades has had arguably the single greatest impact on the world. The invention of the bipolar junction transistor [1] was soon followed by the invention of the integrated circuit [2], light-emitting diode [3], and laser [4]. Semiconductor devices have been the ultimate disruptive technology in history, leading to a re-definition of the state of the art in nearly every field of study. Most impressively this advancement has been not only continuous since the infancy of the semiconductor industry, but also accelerating.

More recently, the field of nanotechnology has brought about a paradigm-shift in the methodology of technical advancement in the semiconductor industry, as well as others. In the past, much effort has been applied to scaling current technologies to smaller sizes. Nanotechnologists take a different disruptive approach by focusing effort on discovering and developing completely new concepts of operation and concepts for fabrication of devices, harnessing natural processes on the smallest of scales. In the regime of nanometer-scale devices, the properties of electronic materials can be very different from the well-known bulk values. The small scale can also allow for previously impossible levels of perfection, and also imperfection, to be attained. Structures can be fabricated that do not contain a single structural defect, or structures can accommodate strains that would cause countless dislocations in a larger version.

One of the structures most intensely studied by nanotechnologists in the semiconductor industry has been the nanowire. Nanowires have been formed by selective-area growth [5], vapor-liquid-solid (VLS) growth [6], etching [7], ablation [8], and other techniques. Many nanowire based devices have been demonstrated including transistors [9], lasers [10, 11], light-emitting diodes (LEDs) [12], solar cells [13, 14, 15, 16, 17], and sensors [18, 19]. Theoretical studies have used nanowires as a test-bed to demonstrate new physics like ballistic transport [20]. New applications for nanowire technology and new device designs are being created through current research efforts, and the possibilities are so vast that much research remains to be done. Sixty years ago, transistors existed only as laboratory experiments, and today it is infrequent that a transistor based device is out of arm's reach. Perhaps the same will be true of nanowires in the decades to come.

1.2 Why a III-V Nanowire?

Silicon is firmly rooted as the king of CMOS, and for good reason. In the early days the ease of growing a high quality oxide on silicon and the fact that its electron and hole mobilities are within an order of magnitude of each other were enough to catapult silicon based BJT and CMOS logic to a dominating position in the semiconductor industry. Since then, advances such as silicon-on-insulator (SOI) [21], strained silicon [22], low-k dielectrics [23], and more recently fin-FET [24] technology have continued to keep silicon the best option for digital and analog integrated circuits in all but a few very specific applications such as extreme radiation tolerance or extremely high frequency amplifiers. However, there are two key qualities that silicon lacks to be the ultimate semiconductor: the ability to efficiently emit light due to its indirect band gap and the ability to form hetero-junctions necessary to design devices for extremely high frequency (>5 GHz). For these types of applications, III-V compound semiconductors have been and remain the answer.

III-V compound semiconductors are the basis for most light-emitting diodes (LEDs), semiconductor lasers, and microwave circuitry in the X-band and higher. Applications range from high-efficiency lighting to the fiber optic communication systems that form the internet to scientific, civilian, and mil-

itary radar systems to communications satellites for television and telephony to non-lethal weapons. In addition, III-V compound semiconductors have found a large market as the higher energy junctions in multi-junction solar cells. The properties of nanowires have been leveraged to propose and demonstrate various next generation III-V devices for the core applications. Single nanowire transistors have been designed that take advantage of the small scale of the nanowire and symmetry useful for gate-all-around type devices. Arrays of nanowires have been integrated into solar cells to improve the light trapping qualities of the cell and eliminate the need for expensive anti-reflective coatings. Light-emitting devices have utilized the quantum confinement characteristics of a small nanowire, or even a quantum well or quantum dot placed inside a nanowire.

Due to the circuit building potential of silicon CMOS, and the optical and high frequency operating potential of III-Vs, it has been of great interest to develop ways to integrate silicon and III-V devices. The long awaited optical interconnects of the future rely on this. Such direct integration has, however, proven to be quite a challenge. Many techniques have been proposed but most suffer from highly defective interfaces between the different materials, or rely on processing that is incompatible for either the III-V or CMOS side of the device. Through their ability to accommodate large strains due to their small size, nanowires show a path towards direct growth of III-V material on silicon or vice-versa. For this reason, combined with the countless novel device designs which have been enabled by nanowire technology, the study of nanowires is justified.

1.3 Organization of the Dissertation

In this thesis, III-V selective area epitaxy grown nanowires (SAE-NWs) are studied and evaluated for use in practical devices. The SAE-NW technique is described and the state of the art in the field is reviewed. Studies on the influence of pattern geometry on SAE-NW growth and the design of SAE-NW p-n junction diodes are presented. Finally, future directions for research on SAE-NWs are presented with results from preliminary experiments.

In Chapter 2, metal-organic chemical vapor deposition and the selective area epitaxy technique are reviewed. Following that, the selective area epi-

taxy based technique for growing III-V nanowires which forms the basis for this entire work is presented in detail. In Chapter 3, progress to date in the field of selective area epitaxy grown nanowires is reviewed. In Chapter 4, a study on the influence of nanowire geometry on growth using the SAE-NW technique is presented. In Chapter 5, results from fabrication of SAE-NW heterojunction diodes are presented with motivation for their use in a nanowire-on-silicon tandem junction solar cell outlined in Section 6.4. In Chapter 6, future directions for the continuing study of the SAE-NW technique are presented with some initial results and thoughts for experiments to be run in the future. In Chapter 7, concluding thoughts are presented.

CHAPTER 2

TECHNIQUES

In this chapter, key techniques are introduced which build upon each other to arrive at the SAE-NW growth process which forms the basis of this work. First, metal-organic chemical vapor deposition (MOCVD) is introduced as the base semiconductor crystal growth technique on which this work is built. After a brief discussion of epitaxy and MOCVD, the concept of selective area epitaxy (SAE) is introduced for both planar and three-dimensional cases. Finally, the selective area epitaxy grown nanowire (SAE-NW) technique is explained as a special case of conventional SAE. Details of the process are presented along with an introduction to hetero-epitaxy of III-V SAE-NWs on silicon.

2.1 Metal-Organic Chemical Vapor Deposition

Modern electronic and photonic devices are predominantly built on single crystal base structures. The process of depositing new material onto a crystal, such that the periodic base structure of the crystal is preserved, is known as epitaxy. During epitaxy, it is possible to grow complex structures involving many layers of different materials if careful attention is paid to the crystal structure and lattice constant mismatch of the dissimilar materials. In this way, through epitaxy a series of layers can be designed such that a particular electronic band structure or optical characteristic is achieved. When a layer of a different material is epitaxially grown on a base material, it is known as hetero-epitaxy. In the most simple case, an interface between two semiconductor layers for which there is a band gap difference or band gap offset can give rise to an electronic potential barrier for carrier confinement while a slight difference in refractive index between the dissimilar layers can give rise to optical confinement. In more complex cases, structures of tens to

hundreds of layers can be designed to form electronic mini-bands and narrow-band distributed Bragg reflectors such as in quantum cascade lasers (QCLs) [25] and vertical cavity surface emitting lasers (VCSELs) [26], respectively.

This work is focused on III-V compound semiconductors, for which multiple crystal growth techniques exist. Some have come and gone, like liquid phase epitaxy (LPE) which was heavily used up until the 1970s [27]. Today, two main crystal growth techniques are used to grow III-V compound semiconductors: metal-organic chemical vapor deposition (MOCVD),[1] and molecular beam epitaxy (MBE). Neither technique has dominated the other because they each fill important niche uses. Material grown via MBE can be higher quality and interfaces between layers can be atomically abrupt. However, the material grown via MOCVD is of more than adequate quality for use in the majority of commercial devices. Additionally, MOCVD growth can be much faster than MBE and the equipment itself is much less expensive to operate. For this reason, MOCVD is used for most mass production of III-V semiconductor devices while MBE is utilized for R&D as well as production of the few devices for which MOCVD would not be acceptable.

Metal-organic chemical vapor deposition is based on the initial work of H. M. Manasevit in 1968 [28]. Since then, several book chapters and dedicated texts have been written on the topic [29, 30, 31, 32, 33]. In MOCVD, growth precursors are passed to a reaction vessel in the vapor phase through the use of a carrier gas. Typically, hydrogen gas is used as the carrier due to the ease of purifying it on site to extremely high levels. This is typically accomplished by diffusing crude hydrogen gas across a palladium-silver alloy membrane at high temperature in what is known as a palladium cell; this process is well known to produce purity in excess of 9N (99.9999999%). Although less common, other inert gases such as nitrogen are used as a carrier as well. Some common precursors are gaseous and can easily be drawn from a cylinder and mixed with the carrier gas for transport to the reactor. However, as the name implies, most of the precursors used are metal-organic (MO) compounds which are typically low vapor pressure liquids or even solids that need to sublimate. These compounds are stored in vessels known as 'bubblers' which are constructed with an inlet dip tube and an outlet from the head space above the liquid or solid fill level. The bubblers are kept in con-

[1]MOCVD is also often referred to as metal-organic vapor phase epitaxy (MOVPE) and organo-metallic vapor phase epitaxy (OMVPE)

trolled temperature water baths to stabilize their vapor pressure at a known point while the dip tube allows carrier gas to be "bubbled" through the liquid or solid source, encouraging evaporation in a controlled manner that is well understood. This vapor/carrier mixture is then pulled off the head space and sent to the reactor vessel. In this way, very controlled amounts of an MO source can be metered and sent to the reaction vessel through the use of a mass flow controller (MFC) measuring the flow of the carrier gas into the bubbler and knowledge of the bubbler temperature.

The vaporized, metered precursors are sent through high purity plumbing to a mixing manifold where valves control the flow of each individual precursor either to the reaction vessel and on to the exhaust, or through a bypass vent which sends the material directly to the exhaust. In this way, carrier gas can run through precursors continually to maintain a stable evaporation rate and switched into the reaction vessel only for the times at which a particular layer is being grown. In the case of thin layers such as quantum wells, this time may only be a few seconds. For MOCVD of III-V materials, often a separate mixing manifold is employed for the Group III and Group V precursors to prevent unwanted reactions before reaching the growth substrate. The growth substrate is heated on a susceptor to temperatures that can range from 400 °C to 1200 °C depending on the material being grown, typically via radiative heating from halogen lights, resistive heating elements, or induction heating using a radio frequency power supply. Pyrolysis of precursors and subsequent reaction with the surface of the substrate results in crystal growth. Reaction vessel pressures range from low vacuum to atmospheric pressure, although a typical pressure is around 100 mbar, which is high enough to achieve reasonably fast growth yet low enough that interfaces between layers can be made abrupt. Reaction vessels themselves are typically made of quartz or stainless steel and can be of either horizontal or vertical topology. The shape of the reaction vessel is specially designed to deliver the precursor to the growth substrate in as even a manner as possible; substrates are also rotated during growth to improve uniformity of the epitaxy.

Common MOCVD precursors are summarized in Table 2.1. Group III precursors are metal-organic compounds; however, Group V precursors are traditionally the hydrides arsine, phosphine, and ammonia. Recent quality improvements in metal-organic group V precursors such as tert-butyl arsenic (TBAs) and tert-butyl phosphorous (TBP) have led to their more widespread

Table 2.1: Typical precursors used in MOCVD of III-V semiconductors.

Name		Group
TMGa	trimethylgallium	III
TEGa	triethylgallium	III
TMAl	trimethylaluminum	III
TMIn	trimethylindium	III
TBAs	tertiarybutylarsenic	V
TBP	tertiarybutylphosphorus	V
TMSb	trimethylantimony	V
N_2H_4	hydrazine	V
MMH	monomethylhydrazine	V
UDMH	unsymmetric dimethylhydrazine	V
AsH_3	arsine	V
PH_3	phosphine	V
NH_3	ammonia	V
SiH_4	silane	IV
Si_2H_6	disilane	IV
CCl_4	carbontetrachloride	IV
CBr_4	carbontetrabromide	IV
DETe	diethyltelluride	VI
DMZn	dimethylzinc	II
DEZn	diethylzinc	II

use and they are preferred in some cases due to their relative safety compared to the extremely hazardous hydrides. Common dopants are mostly metal-organic compounds, but some halides are used. The halogen radicals from halide precursors can actually etch the growth substrate in-situ leading to an effect known as etch-back; care must be taken for good results.

2.2 Selective Area Epitaxy

MOCVD is a powerful technique for growing complex layered semiconductor crystals. Fundamentally though, it is limited to growing uniform layers; each

layer will have a singular ternary/quaternary composition and doping level for its entire extent across the plane of the crystal substrate. Due to this, electronic and optical structure can only be varied in one dimension during growth, in the direction of the growth front normal to the substrate surface. As a result, the structure in the plane of the substrate is added after growth through lithography. For example, a ridge waveguide could be added to an edge-emitting laser for optical mode guiding, or a photonic crystal such as a DBR or two-dimensional lattice of pores might be etched into a laser structure to narrow and tune the emission. This multi-step post-growth-processing can damage the underlying semiconductor and add significant cost to device production.

Selective area epitaxy (SAE) is a technique that can be used to modulate the characteristics of epitaxial thin films in plane during growth; it can be used with both MOCVD and MBE. In SAE, a growth mask is used to prevent interaction of precursors with certain areas of the crystal substrate [34, 35]. This growth mask can be as simple as a one-dimensional stripe [36], a two-dimensional pattern covering a portion of the substrate [37], or a complicated matrix that guides growth in all three dimensions [38]. Results from the first demonstration of 3D epitaxy are presented in Appendix A. An illustration of several types of growth masks is presented in Figure 2.1. The growth mask is typically an amorphous material, such as an oxide or nitride, that can withstand the high temperatures of III-V compound semiconductor growth typical of MOCVD and MBE. PECVD deposited silicon dioxide and silicon nitride are both commonly used. Since there is no chemical reaction between the precursor and the masking material, deposition of material is suppressed in the area of the growth mask.

The effect of the mask on the growth is more complicated than simply blocking deposition of material in the location of the mask; a more interesting enhancement effect takes place. Since precursor material is not being consumed in areas covered by the growth mask, there is a local increase in the precursor partial pressure above masked areas as compared to above a growth surface. As a result, the concentration gradient in the vapor phase causes excess precursor to diffuse to areas adjacent to the growth mask. This results in significantly higher partial pressures of precursor in those locations. Additionally, precursor can adsorb onto the growth mask and the resulting adatoms can diffuse across the surface to a growth front to be incorporated.

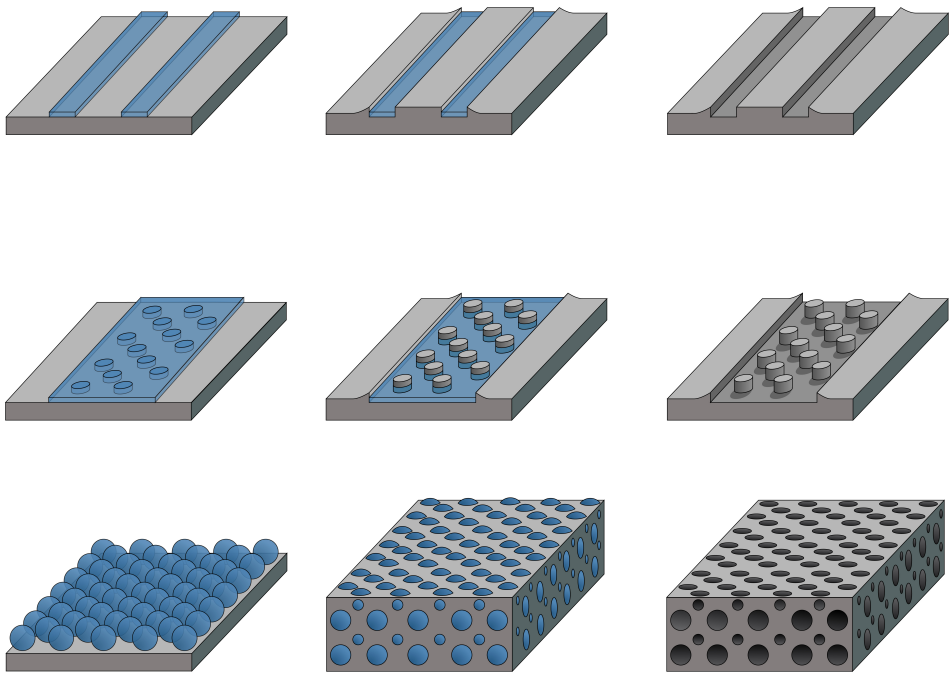


Figure 2.1: Examples of selective area epitaxy masks in 1D, 2D, and 3D. The leftmost column depicts masks as defined on the growth substrate, the central column depicts the result of epitaxial growth around the mask, and the rightmost column shows the growth after the mask has been removed. The top row shows a 1D mask in which a linear strip of material experiences enhancement, the middle row shows a 2D mask in which growth islands experience enhancement, and the bottom row shows a 3D mask where enhancement effects can be quite complicated due to the complex geometry.

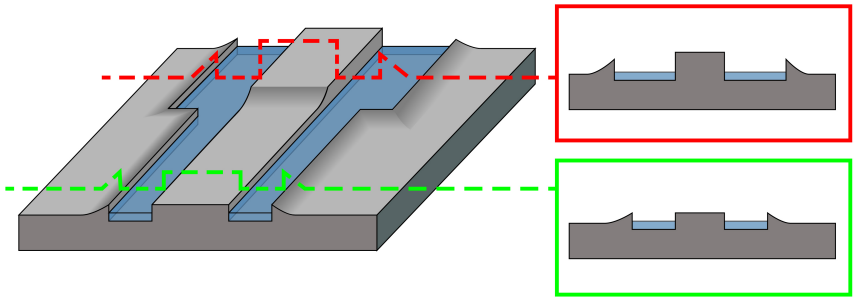


Figure 2.2: The presence of the growth mask causes an enhancement effect which increases the local growth rate, trailing off over a distance of roughly the diffusion length of the precursor in the vapor phase. Note that the wider the oxide strip, the higher the enhancement effect. Enhancement can differ between precursors, leading to varying ternary composition in locations with different mask designs.

The combination of this vapor phase and surface diffusion process leads to an effect known as growth enhancement. Through growth enhancement, material growth rates are increased significantly in a local area. Figure 2.2 depicts a typical selective area growth result.

Since enhancement is essentially due to diffusion processes, the magnitude of the enhancement is dependent on the diffusion constants of the precursors in the vapor phase and of the adatoms on the surface. These diffusion constants can be significantly different for various metal-organic precursors and adatoms, resulting in significantly different enhancement rates for different precursors. This fact is very significant during the growth of ternary and quaternary alloys; the geometry of the growth mask locally changes the composition fraction of such alloys. These effects have been modeled with good agreement with experiment [39]. Through careful mask design and growth condition selection, it is possible to grow different alloy compositions next to each other on the same substrate, enabling entirely new types of device structures to be envisioned.

2.3 Selective Area Epitaxy of Nanowires

The SAE-NW growth technique is a special case of conventional SAE first demonstrated in 2004 [5]. In conventional SAE, although certain common substrate crystallographic orientations and growth conditions are typically used, the technique itself will work over a wide range of substrate orientations and growth conditions. In contrast, the SAE-NW technique uses one particular substrate orientation, (111), and a much narrower range of growth conditions. The combination of the (111) substrate and carefully chosen growth conditions results in the ability to grow a high aspect ratio nanowire structure vertically from the growth mask. In conventional SAE, as the growth extends above the height of the mask, new crystal planes are exposed on the sidewall of the layer which expand outwards to begin to cover the mask. In extreme cases, this can lead to the growth mask becoming completely covered by a coalesced block of semiconductor. This phenomenon has actually been leveraged to great success in the gallium nitride (GaN) material system which suffers from poor quality substrates, and is known as epitaxial lateral overgrowth (ELO) [40, 41, 42, 43]. For a typical SAE device design, however, this lateral growth is undesirable and growth thickness is limited to assure no air gaps are created after mask removal and subsequent regrowth. In the SAE-NW we choose a (111) substrate which, when masked with a pore, will produce hexagonally symmetric {110} planes as sidewalls as the growth front extends above the level of the growth mask. For carefully chosen growth conditions, a large growth rate asymmetry can be achieved between the (111) end facet and {110} sidewall facets. The result is a hexagonal nanowire structure that can grow to aspect ratios in excess of 100 [5, 44, 45]. However, as is common for growth of nanowires on the (111) plane, twin defects are common [46].

Similar to conventional SAE, complex vapor phase and surface diffusion processes affect the growth. However, the presence of additional {110} crystal facets for growth on the sidewalls as well as the evolving three-dimensional topology of the wires during growth is a significant departure from conventional SAE. These effects resulting from evolving geometry of the nanowires are studied in Chapter 4.

The most basic form of the SAE-NW growth process is detailed in Figure 2.3. A (111) oriented substrate is first coated in a thin mask layer, typically

SiO_2 or Si_3N_4, and typically via plasma-enhanced chemical vapor deposition (PECVD). Lithography is then used to define the pattern of pores that will be etched into the mask to define the location and size of the nanowires. Typically electron-beam lithography is used due to the small feature size it can achieve and flexibility in pattern definition; however, other techniques [47] can also be used. Dry or wet etching can then be used to transfer the pattern to the mask layer, at which point the resist is stripped. Figure 2.4 shows an SEM image of a typical EBL defined oxide mask. Following pore definition, a critical step is the definition of the mesa area around the pattern since the size of this mesa will significantly affect the amount of selective area growth enhancement the nanowires will experience. Lithography is once again used to define this mesa, after which the excess masking material is etched away. After stripping the resist that defined the mesa, and a careful post-process cleaning of the sample, MOCVD growth can be performed resulting in the growth of nanowires as shown in Figure 2.5. Conditions for SAE-NW growth are significantly different from those for typical bulk growth on commonly used (100) substrates; typically, the Group III partial pressures are significantly lower and temperatures are higher. These conditions have been shown to provide the highest quality and highest aspect ratio structures [48, 49]. Typical growth conditions for SAE-NWs are presented in Table 4.1 on page 26.

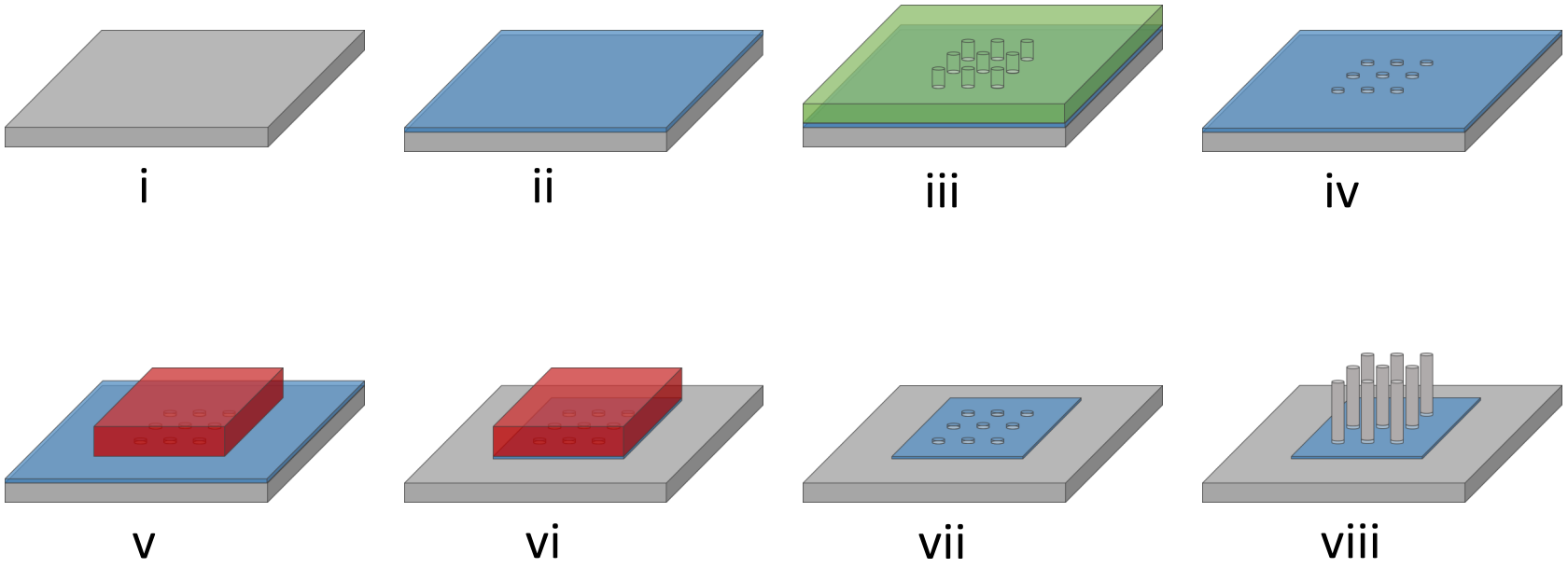


Figure 2.3: The basic SAE-NW growth process. i) A (111) oriented substrate must be used for the SAE-NW process. ii) A dielectric mask is deposited on the substrate, typically SiO_2 or Si_3N_4 via PECVD. iii) PMMA is spin-coated on the sample and the SAE-NW array is defined via electron beam lithography (EBL). iv) A dry or wet etch is used to transfer the EBL pattern to the dielectric mask and the PMMA is stripped. v) A mesa around the pattern is defined via optical lithography so that excess growth mask can be removed resulting in a more controlled and repeatable enhancement level. vi) Excess growth mask is removed via wet or dry etching. vii) Photoresist is stripped and the sample goes through a thorough cleaning process before growth. viii) Growth of nanowires carried out via MOCVD.

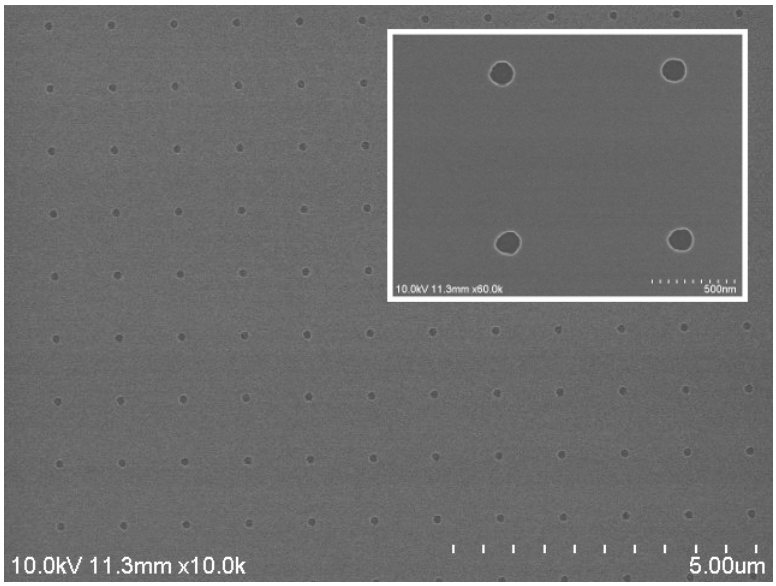


Figure 2.4: An EBL patterned PECVD silicon dioxide mask on a GaAs (111)B substrate ready for growth. Note the circular, non-hexagonal, nature of the pores.

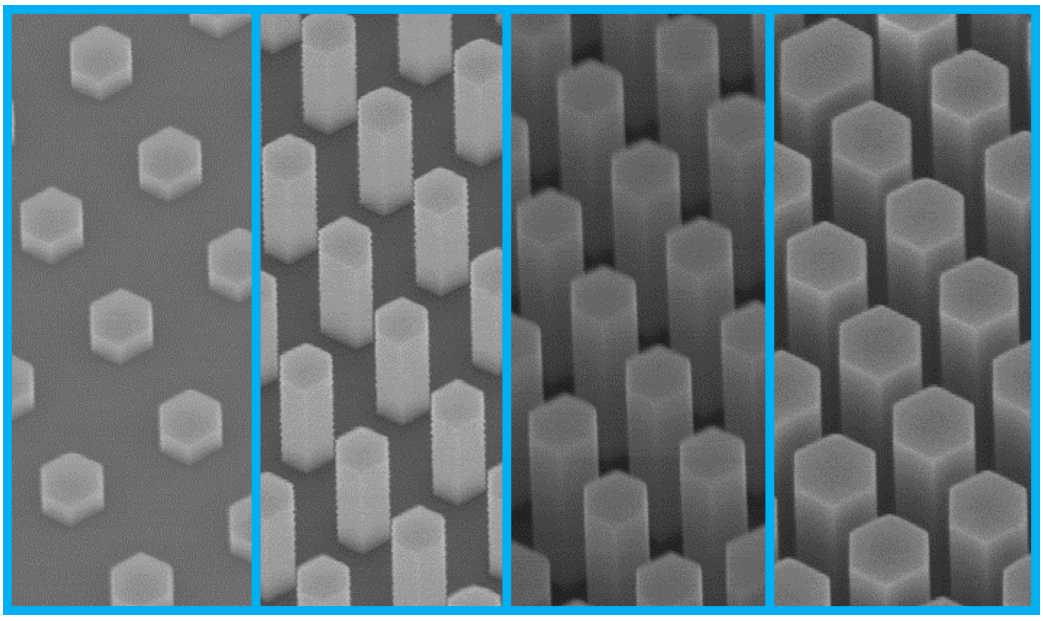


Figure 2.5: SEM images of the evolution of SAE-NW growth. Frames in this series were taken at 20, 40, 60, and 80 minutes of growth time. Note the apparent, yet lesser lateral growth rate in addition to the increased wire length.

CHAPTER 3

BACKGROUND

The SAE-NW technique shows great promise for use in next generation electronic and photonic devices. As such, it has been the subject of significant research effort leading to reports of interesting extensions of the technology and device demonstrations.

3.1 Hetero-Epitaxy on Silicon

During epitaxy, careful attention must be paid to the difference in characteristics between the material that is being grown and the substrate on which it is being grown. Some lattice constant mismatch can be tolerated, but only to a point known as the critical thickness. Regardless, thin film layers grown on significantly lattice mismatched substrates will be strained to compensate, which can significantly change the properties of the material, such as the electronic band gap. Lattice constant mismatch on the order of only a couple percent will result in relaxation of the film through the incorporation of defects at the interface. In cases of extreme mismatch, films will not even be continuous and instead will form randomly self-assembled islands of material. An example of this is shown in Figure 3.1 which depicts the result of GaAs growth on a highly mismatched substrate, silicon. The formation of islands due to the severe lattice mismatch can be seen in Figure 3.1(a). This phenomenon has been leveraged to intentionally form self-assembled nanostructures such as quantum dots. Lattice constants for common III-V semiconductors as well as other semiconductors often used as substrates are presented in Table 3.1.

The SAE technique opens up new possibilities for growth of highly lattice mismatched materials. Through the use of a growth mask, dislocation-free GaAs can be grown in a small local area on silicon, as defined by the mask.

Table 3.1: Lattice constants of common semiconductors [50].

Name	Crystal Structure	Lattice Constant at 300 °K (Å)
Si	Diamond	5.43095
GaP	Zincblende	5.4512
Ge	Diamond	5.64613
GaAs	Zincblende	5.6533
AlAs	Zincblende	5.6605
InP	Zincblende	5.8686
InAs	Zincblende	6.0584
GaSb	Zincblende	6.0959
GaN	Wurtzite	a=3.189 c=5.185

TEM imaging has shown that the GaAs can be dislocation free for up to 10 μm, but the presence of anti-phase boundaries (APBs) indicates imperfect registration of the polar GaAs on the non-polar silicon, which is to be expected. However, for small enough growth areas like those typical in the SAE-NW technique, dislocation-free and APB-free material can be grown [51].

Growth of III-V nanowires on silicon is even more complicated by the polar/non-polar mismatch between epi-layer and substrate than planar or island growth. Nanowires grown out of polar materials will preferentially grow on either (111)-A or (111)-B planes, yet on the surface of a non-polar substrate such as silicon they are presented with four equivalent (111) planes resulting in four possible directions for nanowire growth. Nanowires can grow in random combinations of all four equivalent $\langle 111 \rangle$ directions; however, careful control of growth conditions can suppress the unwanted non-normal nanowire formation [9, 10]. Use of an arsine pre-treatment of the silicon surface during growth of has been shown to generate nearly perfect yield of III-arsenide nanowires normal to the surface of silicon [52, 53] and has been applied to the SAE-NW technique for GaAs [12].

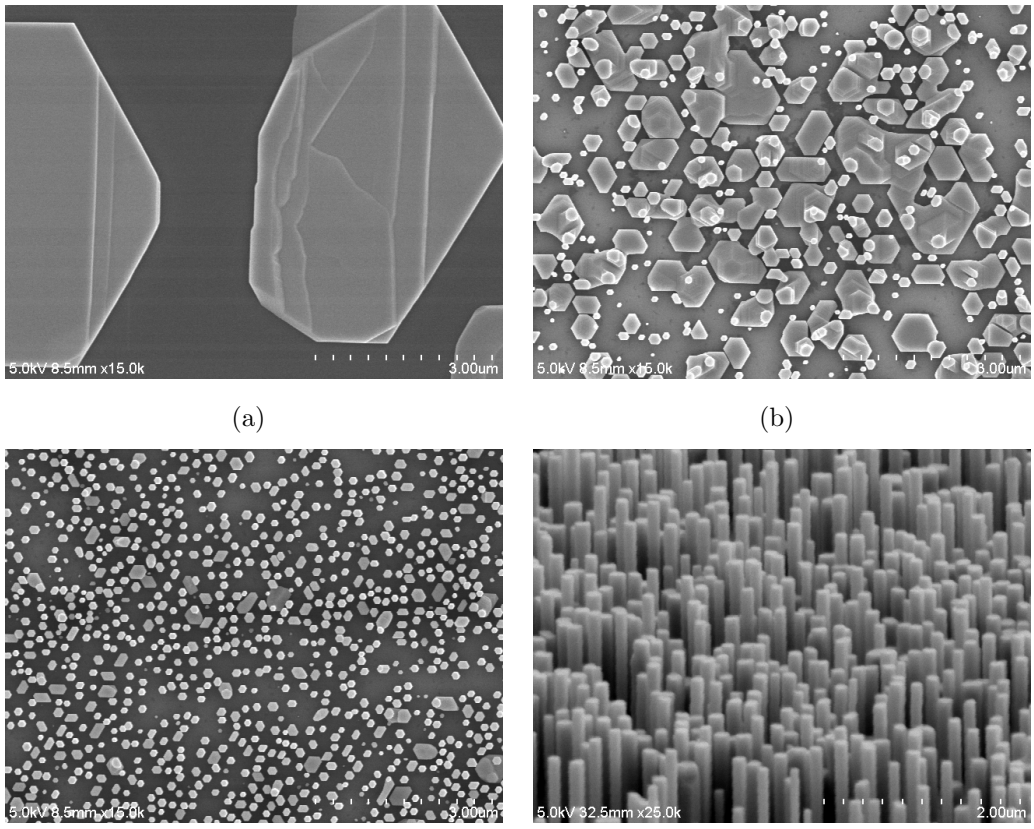
Figure 3.1 shows SEM images of growth in different areas of a SAE silicon substrate. In this particular experiment, the SAE mask was overetched an damaged, which yielded an opportunity to observe the morphology of the growth in areas of varying oxide thickness and quality. In areas outside

the SAE mask, where the native oxide has been thoroughly removed, large areas of bare silicon are exposed. In these areas, large islands of GaAs are formed during growth as shown in Figure 3.1(a). In areas where the oxide is mostly intact, but still discontinuous with a large number of pinholes, SAE-NW structures begin to be visible growing from pinholes as shown in Figure 3.1(c)-(d). In areas between the bare silicon and where the mask is present but discontinuous, a patchy area exists where the mask has been mostly removed but some areas of pinhole containing mask still exist. This induces growth of a combination of medium sized islands and SAE-NW structures as shown in Figure 3.1(b).

Devices based on the hetero-epitaxy of III-V compound semiconductors on silicon have been demonstrated, including a SAE-NW LED discussed in Section 3.2.

3.2 Light Emitters

Optical characterization of SAE-NWs has been reported, including studies of core shell structures and embedded quantum wells [54]. Electrically injected devices have been demonstrated, including a light-emitting diode (LED) using a core multi-shell (CMS) design in which AlGaAs shells surrounded an inner GaAs shell to provide heterostructure confinement. The CMS structure was realized by first growing GaAs core nanowires using the SAE-NW technique and then changing the growth conditions to grow conformal shells in sequence. After deposition of metallic top contacts using a rotation holder so as to coat both the top and sides of the nanowires, a mechanical polishing technique was used to remove metal from the top so as to leave a contact that makes electrical contact only on the sidewalls of the nanowire, allowing for vertical light emission [12]. Separately, observation of Fabry-Pérot modes in SAE-NWs has demonstrated that optical cavities necessary for lasers can be realized [55, 56]. These demonstrations have established important milestones such as successful electrical injection of a III-V SAE-NW light emitter integrated onto a silicon substrate, and formation of an optical cavity. Together, they represent a path towards realistic integration of III-V optical emitters, including lasers, into CMOS processes.



(a) (b)

(c) (d)

Figure 3.1: (a) Growth in areas of bare silicon where the native oxide has been completely etched away results in large islands. (b) In some areas between those where the oxide is completely etched and remains, a combination of large island growth and nanowire growth is observed. (c) In areas where the oxide remains, but is etched to the point of being extremely thin and porous, nanowires grow from defects in the oxide. (d) A tilted view of the wires in (c).

3.3 Sensors

Photo-detectors are an important part of any optical communication system, as well as optical sensor systems. Nanowire based photo-detectors are attractive due to the enhanced light absorption that can be achieved through light trapping [57]. Photo-detectors based on GaAs SAE-NW arrays with transparent indium tin oxide (ITO) top contacts have been demonstrated [19, 18]. Results have shown promise for operation of these devices as part of a high speed optical communication link due the photo-detector array's low capacitance and operation at low bias [18].

Another promising area of nanowire based device development is surface-functionalized bio-sensors and chemical detectors. Although there have been numerous demonstrations of nanowire devices of this sort [58], there has not been a single demonstration of a surface-functionalized SAE-NW based device to date. Leveraging the inherent benefits of the SAE-NW technique for the purpose of surface-functionalized devices represents a significant untapped opportunity in the SAE-NW research community.

3.4 Solar Energy Conversion

Nanowire arrays can improve solar energy conversion devices including photovoltaic cells for production of electricity and photo-electrolysis cells for the production of hydrogen fuel. Through consideration of scattering in the nanowire array, proper design can lead to extremely low reflectivity over a broad spectrum and improve the absorption of light and therefore efficiency of devices [57]. Other benefits of the use of a nanowire array include better carrier separation and lower material use, but these do not come without significant drawbacks such as increased recombination due to the larger surface area [59].

To date, nanowire solar cells have been demonstrated with an impressive 13.8% efficiency [13]. Although that demonstration utilized Au-catalyzed VLS growth, solar cells based on SAE-NWs have also been demonstrated [15, 17, 16]. Designs for tandem junction nanowire-on-silicon solar cells have been proposed, and analyzed theoretically to have a limiting efficiency of 38.8% at 1 sun illumination and AM1.5 G [60]. Work has also been published

on optimization and current matching in tandem junction nanowire-on-silicon solar cells [61]. To date, a tandem junction nanowire-on-silicon solar cell has not been reported. An important step towards such a device is the development and characterization of a tunnel diode to form the connection between the nanowire cell and planar cell. Development of an appropriate tunnel diode for this purpose is the focus of Chapter 5. More details on the design of a tandem nanowire-on-silicon solar cell are presented in Section 6.4.

The same light trapping and carrier collection characteristics that make nanowire arrays attractive for photo-voltaic cells also make them attractive for solar water spitting applications when used as the electrode in a photo-electrolysis cell [62]. Nanowire photo-anode arrays grown via the SAE-NW technique have been studied for this purpose and shown promise for use in dual-junction III-V nanowire on proposed silicon solar water splitting systems [63]. Although a device has yet to be demonstrated, SAE-NWs could form an integral part of future photo-electrolysis cells for renewable production of hydrogen for fuel.

3.5 Photonic Crystals

The inherent lithographic control of nanowire diameter and location in the SAE-NW technique opens up the possibility of fabricating SAE-NW based photonic crystal devices. Photonic crystal cavities and optically pumped lasing have been reported using the SAE-NW technique [64, 11]. However, in these demonstrations the nanowire arrays had to be removed from the growth substrate to improve out-of-plane confinement and limit optical guiding into the substrate. By removing the nanowire photonic crystals from the substrate, the possibility to directly grow a photonic integrated circuit on a CMOS chip, the greatest advantage of the technique, is lost. A potential process to alleviate this issue and allow for integration of SAE-NW based photonic crystal components onto a CMOS chip is outlined as a possible future experiment in Section 6.3.

CHAPTER 4

EVOLUTION OF GAAS NANOWIRE GEOMETRY IN SELECTIVE AREA EPITAXY

Nanowires (NWs) grown via selective area epitaxy (SAE) show great promise for applications in next generation electronic and photonic devices, yet the design of NW-based devices can be complicated due to the complex kinetics involved in the growth process. The presence of the patterned selective area mask, as well as the changing geometry of the NWs themselves during growth, leads to non-linear growth rates which can vary significantly based on location in the mask and the NW size. Here we present a systematic study of the evolution of GaAs NW geometry during growth as a function of NW size and pitch. We highlight a breakdown of NW uniformity at extended growth times, which is accelerated for NW arrays with larger separations. This work is intended to outline potential fundamental growth challenges in achieving desired III-V NW array patterns and uniformity via SAE.

4.1 Introduction

Semiconductor nanowires (NWs) grown by the selective area epitaxy (SAE) technique have recently been shown to be promising for various photonic and electronic device applications [63]. Many SAE-NW-based devices have recently been demonstrated including photonic crystal cavities [64], Fabry-Perot resonators [56], lasers [11], photo-detectors [18, 19], and various solar cell designs [17, 16, 15]. In addition, research demonstrating the direct growth

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of compound semiconductor SAE-NWs on silicon has shown a pathway to direct integration of photonic devices onto CMOS chips, possibly providing a much sought after solution to a long standing technical challenge [12, 51]. A major advantage of the SAE technique over other growth methods is the inherent lithographic control of the location and size of the wires; making it possible to design site-controlled, array-based devices. Furthermore, the SAE approach circumvents notable challenges associated with Au-mediated vapor-liquid-solid (VLS) NW growth, such as morphological non-homogeneity [65], phase-segregation in ternary/quaternary alloys [66], and Au precipitant contamination [67].

Many NW-based device demonstrations have involved NWs randomly located on a sample due to the nature of the self-assembly process [14, 68, 69]. This presents a challenge for integration and makes precisely ordered arrays, necessary for some device designs, impossible. The SAE-NW technique can solve this issue by using a lithographically defined growth mask to precisely locate and control the size of the wires. However, the presence of the growth mask required in the SAE approach causes an enhancement of epitaxial growth in the local area around the growth mask due to surface diffusion, a well-known phenomenon in thin film SAE [27, 37]. Since the presence of the mask modulates the local partial pressure of precursors in a given growth area on the substrate, local enhancement can vary between different growth species due to their different diffusion properties, resulting in locally varying ternary and quaternary compositions [39]. In addition to these common SAE effects, the SAE-NW technique suffers from additional complications due to the increased surface-area-to-volume ratio and introduction of large sidewall facets during growth. The geometry of the NW array itself can also cause a relative enhancement in a local area due to dynamic vapor phase diffusion and adsorption processes. Both of these departures from conventional thin film SAE will be discussed in relation to experimental results in this work. Additionally, the SAE-NW growth process may not be completely selective along the NW axial direction and the existence, although small, of a competing growth mode on the {110} sidewalls of the NWs cannot be completely ignored in order to precisely predict the final dimensions of a NW-based periodic array, and is even further complicated in the case of aperiodic arrays (i.e., photonic crystal waveguides and defect cavities). The combination of these factors motivates an in-depth study to further the understanding of

the complex growth process. In this work we present a systematic study of SAE-based GaAs NW growth and quantify the effect of the selective area mask pore size (D_P) and pitch (a) on the evolution of the wires.

We have observed that while radial growth of NWs remains roughly constant and linear with time, axial growth exhibits a trend in which a slower initial growth regime precedes a linear, steady-state growth regime, in which the growth rate trails off. Since pattern geometry and resulting NW morphology vary significantly for the structures studied, we also present volumetric analysis of the growth data. Through volumetric analysis, it can be seen that the rate of material volume addition is nearly constant over the changing pattern geometry, with a slight variation in volume addition rate with time, explained by variable onset of the saturation region based on pattern geometry. Hexagonal geometry is shown to break down, likely due to synergetic growth effects [70] once a threshold is reached, eventually turning a NW array into a coalesced block. This threshold depends on the enhancement ratio of a given pattern and the spacing between NWs. This work highlights the growth window conducive to the synthesis of NW arrays with perfectly hexagonal geometries, and shows the challenges associated with SAE beyond these boundaries.

4.2 Experimental Details

Selective-area epitaxial growth masks were made by depositing 20 nm SiO_2 onto GaAs substrates via plasma-enhanced chemical vapor deposition (PECVD), followed by lithography to define the growth mask, which was carried out on a Raith e-line electron-beam lithography system. Growth templates consisted of 100 μm $\times$ 100 μm arrays of pores with an oxide skirt size (mesa) of 400 μm $\times$ 400 μm. Arrays varied in pore diameter from 125 nm to 225 nm (50 nm incremental), and in pitch from 1 μm to 0.6 μm (100 nm incremental). The constant array-to-oxide skirt size was chosen to eliminate enhancement effects for all samples studied. An example of the mask pattern prior to growth is shown in Figure 4.1.

Growth was carried out in an AIXTRON AIX-200/4 MOCVD system. Trimethyl-gallium (TMGa) and arsine (AsH_3) were used as group-III and group-V precursors, respectively. Nanowire growth was performed at

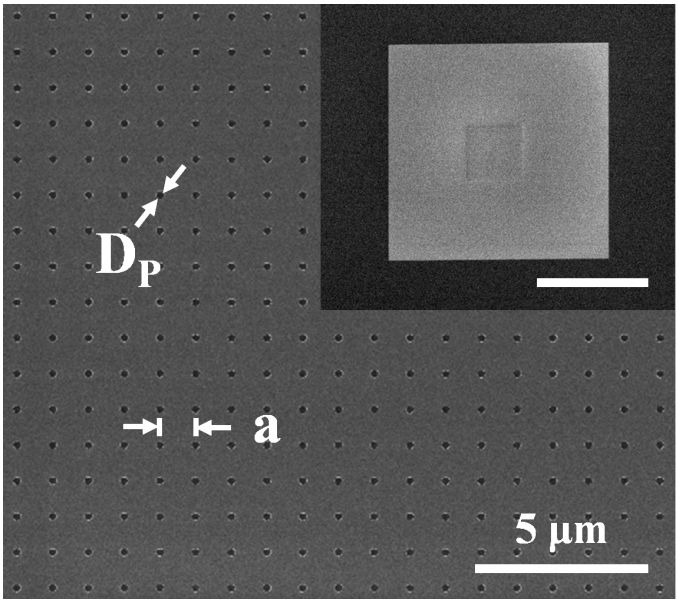


Figure 4.1: Plan-view SEM image of pattern area showing the square lattice of pores. Pore diameter and pitch are labelled as D_P and a, respectively. Inset shows a SEM image of a 100 μm × 100 μm electron-beam lithography patterned array of pores in a 400 μm × 400 μm SiO_2 mesa (inset scale bar represents 200 μm).

750 °C at 50 mbar total pressure with palladium-diffused hydrogen (H_2) as the carrier gas. A native oxide desorption step was carried out at 800 °C under a constant AsH_3 flow. The total growth time was 80 minutes, broken into four consecutive 20 minute growths, after each of which, observations were made via scanning electron microscopy (SEM) using a Hitachi S-4800. It should be noted that the above growth conditions are representative of a comparable parameter space as previous reports on SAE-grown GaAs NWs, as presented in Table 4.1.

4.3 Results and Discussion

Unity NW growth yields are achieved (i.e., every pore leads to a vertical GaAs NW) over all the arrays investigated, as shown in the supplementary material [71]. Examples of the resulting NWs grown by the SAE method are shown in Figure 4.2. All frames of Figure 4.2 were taken after growth step 2 (t = 40 min). The top pair of rows shows plan-view and 30° tilted-view SEM

Table 4.1: Comparison of the growth conditions for this study to other published work on SAE-grown GaAs NWs. Note for core-shell or QW/QD structures only the base GaAs NW is considered.

	Growth temperature (°C)	Pressure (atm)	TMGa partial pressure (atm)	AsH_3 partial pressure (atm)	V/III Ratio
This work	750	0.097	2.7×10^{-6}	2.5×10^{-4}	93
Hokkaido	750	0.1	2.7×10^{-6}	2.5×10^{-4}	93
Hokkaido	750	0.1	2.7×10^{-7}	2.5×10^{-4} to 1.7×10^{-3}	926-6296
Hokkaido	700-850	0.1	2.7×10^{-6}	2.5×10^{-5} to 5.0×10^{-4}	9.3-185
Hokkaido	750	0.1	2.7×10^{-6}	5.0×10^{-4}	185
Hokkaido	750	0.1	8.2×10^{-7}	2.5×10^{-4}	305
UCLA	735	0.79	...[a]	...[a]	...[a]
UCLA	720	0.79	...[a]	...[a]	9
USC	700	0.1	3.8×10^{-7}	7.1×10^{-5} to 2.4×10^{-4}	189-643
USC	760	0.1	7.6×10^{-7}	2.1×10^{-4}	283
USC	790	0.1	3.7×10^{-7}	4.8×10^{-5}	127

[a] Undisclosed information

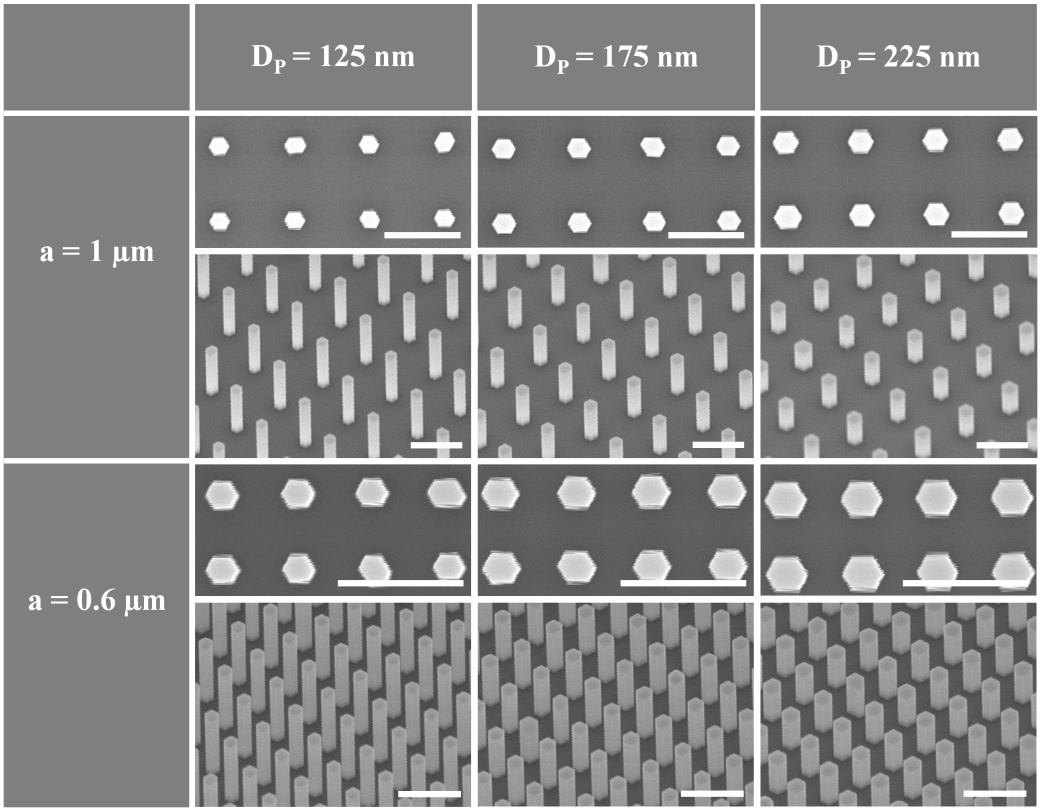


Figure 4.2: Plan-view and 30° tilted-view SEM images of SAE-grown GaAs NWs. Patterned pore diameter varies across columns: 125 nm, 175 nm, 225 nm. The second and fourth rows are tilted views of the first and third rows. D_P and a define the lithographically patterned pore diameter and pitch, respectively. Pitch varied from 1 μm in the first row to 600 nm in the third row. Note that the magnification varies in all rows. However, all scale bars are 1 μm.

images of the largest array pitch (1 μm), while the bottom pair of rows shows the same for the smallest array pitch (600 nm). As expected, and seen in the tilted-view panels in Figure 4.2, an inverse proportionality exists between NW length and pore diameter. This will be explored in detail with regard to volumetric growth conservation below. We further note that epitaxial registry exists between the substrate and the NWs (vertical NW growth is found on a (111)B surface) and that hexagonal NW symmetry is preserved with parallel {110} oriented sidewall facets observed amongst neighboring NWs.

The evolution of NW geometry with time is shown in Figure 4.3. Thirty degree tilted-view SEM images of the same pattern across the four growth

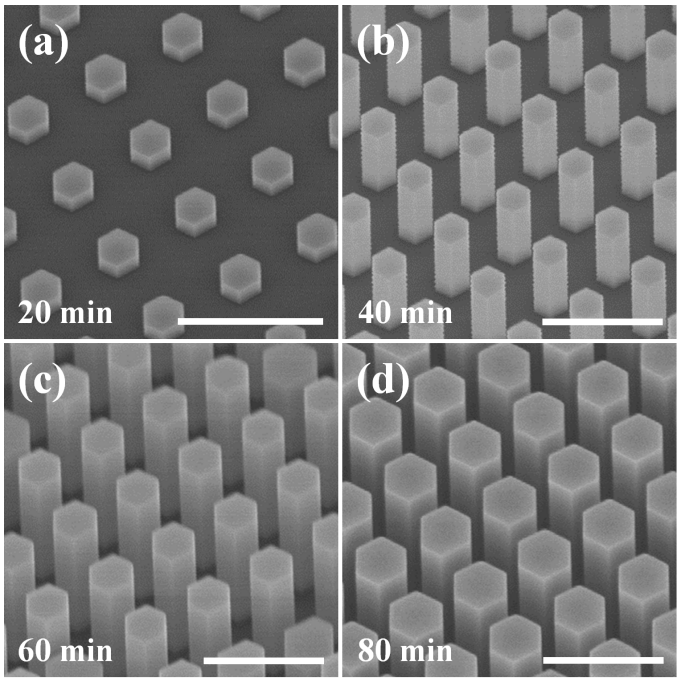


Figure 4.3: 30° tilted SEM images of the time evolution of NW geometry over the four growth steps (t = (a) 20, (b) 40, (c) 60, (d) 80 min) for a 600 nm pitch and 225 nm diameter pore array. All scale bars represent 1 μm.

steps are shown. To eliminate sample-to-sample patterning variation, and for self-consistency, the initial growth was followed by three re-growth steps on the same template. In addition to the desired axial growth of the NWs in time, the smaller, yet non-trivial, radial growth can also be clearly observed as evidenced by the reduced gap between nearest neighbor NWs. This trend will be quantified later in the discussion of detailed measurements presented in Figure 4.4. To quantify crystal growth evolution trends, NW lengths and diameters were measured via SEM after each of the four growth steps. Every data point represents an average value taken from at least 10 individual NWs, with error bars showing the approximate maximum and minimum deviation range from the mean. Large area analysis demonstrated consistent growth trends as compared to the smaller sample sets measured. An image processing program [72] was used to measure and average the area of the end facets of the NWs. Diameter was defined as the length across a perfect hexagon from point to point with equivalent area, by use of Equation 4.1.

$$D_{PerfectHexagon} = 2 \times \sqrt{\frac{2}{3 \times \sqrt{3}} \times A_{Measured}} \tag{4.1}$$

The use of this calculation allowed us to meaningfully assess the addition of material volume across growth steps as perfect hexagonal symmetry began to break down. Simply measuring the Feret diameter of the NWs as they evolve and become less symmetric would not yield an accurate NW volume once those Feret diameters were used to calculate hexagonal area and multiplied by length. The resulting measurements of length and diameter are plotted in Figure 4.4.

In the final region, saturation of the axial growth rate begins. While the slow growth rate experienced in the first growth regime could be explained as a growth nucleation effect, this nucleation phase also exists before each growth step, as the same sample was re-grown for each data set. Instead, the growth is actually limited by the initially small surface area of the pores that are unable to capture all available growth species before they diffuse to adjacent unpatterned growth areas, which act as a large material sink. Once the NWs reach some initial length, they have sufficient surface area to fully capture all the limiting material precursors before they diffuse away. Once this minimum surface area is reached, the maximum axial growth rate is reached in turn, and the main linear growth regime begins. This linear growth continues until the radial expansion of the wires reaches a point at which gaps between the wires start to limit diffusion in the gas phase to the sidewalls. At this point, the effective surface area of the NWs in the array for adsorbing precursors from the gas phase starts to decrease, leading to lower effective growth rates. Although the above length and diameter evolution trends, shown in Figure 4.4(a), are useful for targeting specific NW geometries, they show an incomplete view of the overall selective area growth kinetics. For a more complete picture, we are interested in understanding the evolution of NW volumes during SAE. In Figure 4.4(b) and 4.4(c) the average NW volume vs. time and corresponding volumetric growth rate vs. time are plotted, respectively. In Figure 4.4(b) we note an exponentially increasing trend at each time interval, indicating an accelerating volumetric growth rate. This is a significant observation, which differs dramatically from the linear growth trend of conventional two-dimensional (2-D) film SAE. The prominent difference between 2-D SAE and NW-SAE is the constant geometry of the former

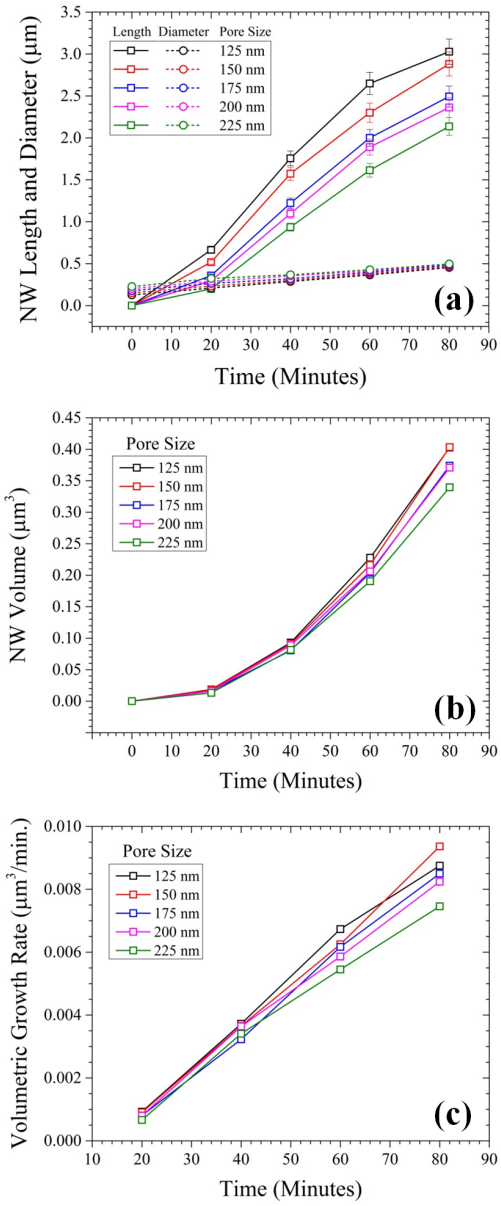


Figure 4.4: (a) Plot of NW length and diameter vs. growth time for patterns with a 600 nm pitch. Error bars represent the maximum and minimum deviation from the mean (smaller deviation values are hidden data points). The radial growth rate is significantly smaller than the axial growth rate as expected for SAE NW growth. However, note that the radial growth rate is not zero (4.1 and 2.9 nm/min for 125 and 225 nm pores, respectively) and is approximately linear, in contrast to the non-linear axial growth. (b) Plot of NW volume vs. growth time for patterns with a 600 nm pitch as calculated from measurements of length and cross-sectional area via SEM. (c) Plot of NW volumetric growth rate derived from the data of (b). Note the linearity of the plot indicating constant volume addition to the NW with time.

and the variable geometry of the latter, which introduces new surfaces for material capture as growth continues. Whereas for planar SAE structures, a constant exposed area exists for nucleation of vapor-phase growth species, the material sink for NW geometries is continually increasing through the introduction of actively expanding surfaces that can capture diffusive adatoms. Within the parameter space explored in the current study, NW growth evolution is not simply limited by surface diffusion of growth species, nor by the supply of adatoms from the surrounding vapor phase. Rather, the most influential factor that determines NW volumetric growth is the geometry of the individual NWs comprising the array. Based on previous NW-SAE reports for InAs [73], we should expect to exit the geometry-limited regime and enter a surface diffusion-limited regime in which volumetric growth rate becomes constant at extended growth times. However, as supported by Figure 4.4(c), our volumetric growth rate is monotonically increasing for all time intervals and pore sizes. The current increasing growth rate trend can be justified by considering the diffusion length discrepancy between In and Ga, since the onset of a diffusion-limited growth regime, relative to one that is geometry-limited, is expedited for shorter diffusion lengths.

Under the conditions explored here, an even more dramatic evolution in NW growth is observed prior to the onset of diffusion-limited volumetric growth rate saturation; namely, the breakdown of NW hexagonal symmetry. As growth evolves, the hexagonal symmetry of the NWs begins to degrade in patterns where the gaps between NWs have decreased due to the radial growth. Such a geometric breakdown effect is quantified in Figure 4.5, where hexagonally symmetric NW yield (fraction of NW grown with equilateral hexagonal cross-sections) is plotted as a function of growth time. We note that as the growth time increases, the yield of hexagonally symmetric NWs decreases such that, in the most extreme scenario, only 60% of all NWs in an array have preserved their original geometries. The tilted-view SEM images shown as insets in Figure 4.5 demonstrate the noted breakdown phenomenon, which can likely be attributed to synergetic growth effects [70] arising from substantial radial growth (reduced nearest neighboring NW distance) at extended growth times. This can become a runaway effect, eventually filling in the entire array and forming a large coalesced block. Further validation of the synergetic growth phenomenon is presented in the supplementary material [71]. Asymmetric NW growth at extended periods was not observed to

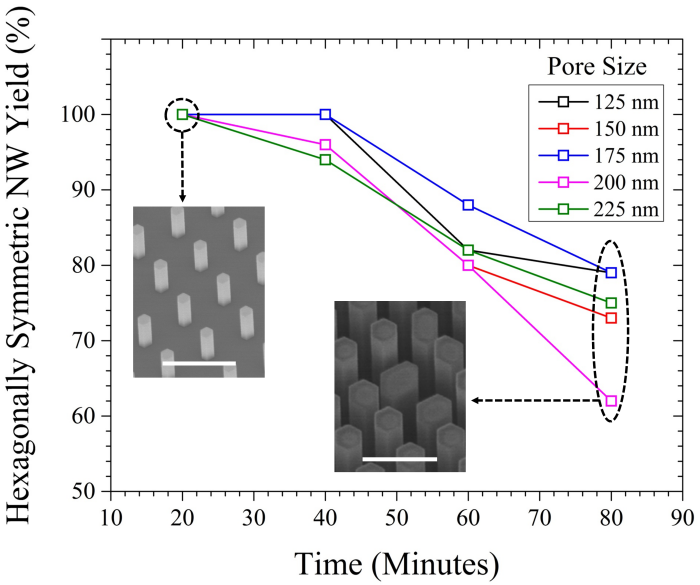


Figure 4.5: Measured yield of hexagonally symmetric NWs as a function of growth time. Insets show representative tilted-view SEM images of as-grown NW arrays with identical pore diameter (D_P = 125 nm) and pitch values (a = 600 nm) after 20 minutes (left) and 80 minutes (right) of growth. Inset scale bars represent 1 μm.

vary along the length of the NWs. As such, symmetry breakdown did not result in the formation of NWs with tapered geometries. Lastly, it should be noted that since SAE NW growth evolution depends strongly on the pitch of pore patterns, such that growth rate trends are exaggerated for larger pitch values, breakdown of hexagonal symmetry was observed at shorter growth times for pitch values greater than 600 nm. As such, our systematic study of growth trends was limited to patterns with P = 600 nm.

High-resolution transmission electron microscopy analysis reveals that NWs grown under these conditions exhibit a polytypic crystal structure composed of a predominant zinc-blende lattice with high density incorporation of lateral stacking faults. Room-temperature photoluminescence (PL) spectra taken from these NW arrays show strong emission centered at ~870 nm along with resonant cavity mode-like peaks, implying good optical quality of the NWs. Further analysis of both the TEM and PL results will be reported separately. In summary, we have presented an in-depth study of GaAs NW growth evolution via SAE. Examinations of growth rate trends based on systematic growth studies allowed for an understanding of the complex growth kinetics

present during III-V NW-SAE, and provided insights into the capabilities and limitations inherent to the technique. An analysis of NW growth rate based on volume allowed us to establish the prevalence of a geometry-limited growth regime prior to the onset of diffusion-limited growth. Furthermore, a breakdown of hexagonal symmetry in NW cross-section was observed for a combination of sufficiently high growth enhancement and narrow gap between adjacent wires. Knowledge of the ideal growth boundaries, which define the limits before the onset of growth homogeneity breakdown, will aid in future device designs where a perfect hexagonal NW morphology is highly desirable. These guidelines for symmetrically hexagonal NW growth and defective growth mitigation techniques may be adopted based on these findings to either discourage or encourage the formation of coalesced structures as the device designer intends. The trends presented herein should provide direction for device designers targeting specific SAE-NW geometries for applications in a myriad of active and passive device designs.

CHAPTER 5

HETEROJUNCTION DIODES—TOWARD TANDEM NANOWIRE-ON-SILICON SOLAR CELLS

5.1 Introduction

The SAE-NW technique is very promising for use in tandem junction III-V on silicon solar cells. Since it is impossible to directly grow a high quality III-V layer directly on silicon due to lattice mismatch, exotic techniques have been explored to solve this problem including a novel fusion bonding technique [74]. A better solution is to leverage nanowire growth techniques, such as SAE-NW growth, which allows for highly lattice mismatched materials to be integrated. Studies have shown that a III-V nanowire-on-silicon tandem junction solar cell has an impressive 38.8% limiting efficiency [60]. If such a device can be realized, it will likely surpass state-of-the-art single crystal single junction silicon solar cells in the commercially key metric of cost per watt. There are three main challenges to harnessing the SAE-NW technique for this purpose: fabricating a high quality solar cell out of a III-V nanowire, growing that III-V nanowire on a silicon substrate, and forming a tunnel diode junction at the interface between the nanowire and silicon. The first two challenges have been overcome; nanowire solar cells have been fabricated using SAE-NWs [16, 15] with others achieving impressive efficiency [13] and growth of III-V SAE-NWs on silicon has been demonstrated [12, 53]. Although an InAs on silicon tunnel diode has been demonstrated [75], it is not useful in a multi-junction solar cell since it is not transparent in the necessary spectrum due to its low band gap. Therefore, the third challenge remains. In this work, we fabricate heterojunction diodes by growing SAE-NWs on silicon substrates to study doping at the high levels necessary for a tunnel junction. We identify an interesting dispersion in the Zener breakdown and highlight a path to a tunnel diode.

Tunnel diodes were discovered in 1957 at Sony [76]. Initially they were

considered interesting for the negative differential resistance they exhibit, and were used in state-of-the-art high frequency oscillators for radio applications. Today they are critical to the function of multi-junction solar cells. A tunnel diode is essentially an abrupt p++/n++ junction. Due to the extremely high doping in the p and n layers the depletion width of the junction is very small, typically ten nanometers or less. At equilibrium, since the separation between the carriers on either side of the depletion region is so small, electrons can tunnel between the conduction band of the n region and the valence band of the p region. Application of a small potential in either direction, thus driving the quasi-Fermi levels apart slightly, will result in current flow. As increasing reverse bias is applied and the quasi-Fermi levels are driven farther apart, more and more states overlap allowing a larger and larger current to flow in the reverse direction. As increasing forward bias is applied, more and more states overlap allowing the forward current to increase. This continues to the point at which the conduction band in the n region is biased above the quasi-Fermi level in the p region, causing the overlap of states to begin to decrease and giving rise to the characteristic negative differential resistance (NDR) observed in the forward bias region. After sufficient forward bias has been applied, tunneling ceases and a normal rectifier forward characteristic is observed.

As mentioned earlier, tunnel diodes are used in two primary applications: oscillators, and multi-junction solar cells. In these applications, however, they are actually used in opposite ways. High frequency oscillators are designed taking advantage of the NDR region in forward bias whereas multi-junction solar cells take advantage of the reverse tunneling current to pass carriers from the conduction band of one sub-cell to the valence band of the adjacent sub-cell. In this way subsequent sub-cells in a multi-junction stack can be connected. Incident photons on the first cell will excite an electron to the conduction band. In this way, the open circuit voltages of the cells add in series. Since the sub-cells are connected in series, careful attention must be paid to matching the photo-currents produced in the sub-cells for an efficient and reliable device [61].

5.2 Experimental Details

Although a nanowire-on-silicon solar cell would require a ternary alloy to achieve the optimal band gap of 1.7 eV[1], ternary alloys add significant complication to experiments by adding a significant variable. This is especially true for the SAE-NW technique where precursors can be differentially enhanced and multiple crystal facets are exposed during growth. For this reason, GaAs was used as an analog material in this study to investigate the feasibility of fabricating a tunnel junction for a nanowire-on-silicon solar cell. GaAs is a good analog since the addition of a moderate amount of phosphorus (∼23%) yields the proper band gap, in a material with similar growth characteristics and identical dopant species to pure GaAs. Once the doping of the diode junction is well understood, movement to GaAsP is not expected to create additional complication.

Diode structures were fabricated by growing heavily p-doped GaAs SAE-NWs on heavily n-doped silicon substrates. The details of the process for definition of the SAE growth masks is described in Section 4.2. Similar to that study, 100 μm × 100 μm nanowire arrays were defined in the middle of 400 μm × 400 μm oxide skirts (mesas). In contrast, all pore diameters were 100 nm and pitch varied from 1 μm to 0.5 μm (250 nm incremental). Substrates were prime grade (111) oriented n-type silicon doped with arsenic, specified by the manufacturer to have a resistivity in the range of 2.0 to 5.0 mΩ-cm. In addition to the standard SAE-NW processing steps described in Section 2.3, a pre-growth dip in 50:1 buffered oxide etchant (BOE) was used to remove the native oxide on the silicon immediately before growth. After a brief rinse and nitrogen blow dry after etching, the samples were quickly transferred to the nitrogen glove-box load-lock on the MOCVD tool. Nanowire growth was carried out in an AIXTRON AIX-200/4 MOCVD system with TMGa and AsH_3 as Group III and Group V precursors. Two p-type dopants were utilized: diethylzinc (DEZn) and carbontetrabromide (CBr_4). Nanowires were grown at 750 °C and at 50 mbar reactor pressure with a palladium-diffused hydrogen (H_2) carrier gas. A brief oxide desorption step under arsine overpressure at 850 °C preceded growth. A Hitachi S-4800 scanning electron microscope (SEM) was used to inspect the nanowire morphology and deter-

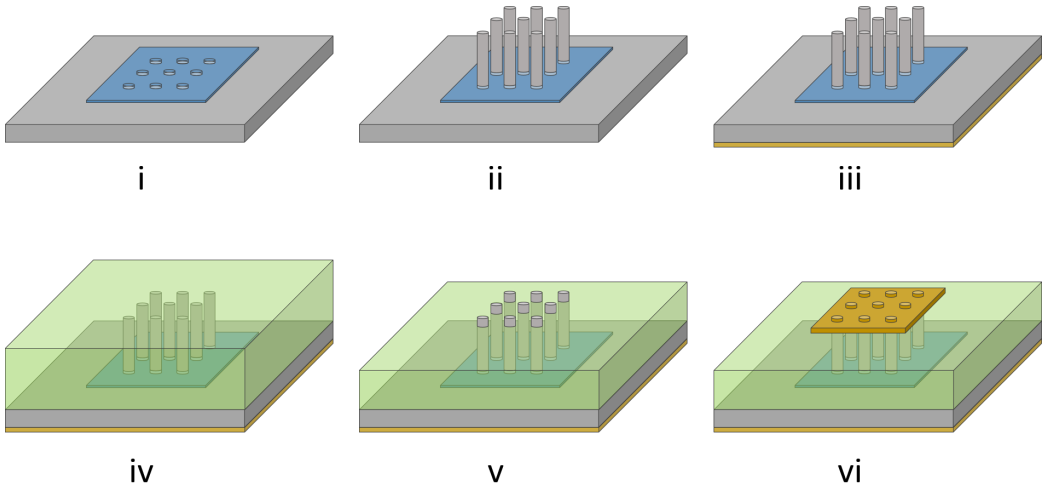
[1]Band gap of 1.7 eV is based on an optimal tandem cell for AM1.5 G assuming the lower sub-cell is silicon

mine height. Unity nanowire yields were observed; however, some growths resulted in slightly less than unity yield arrays likely due to a heater failure which limited the desorption temperature ramp rate for a series of growths. In those growths, the desorption step did not reach the intended temperature of 850 °C.

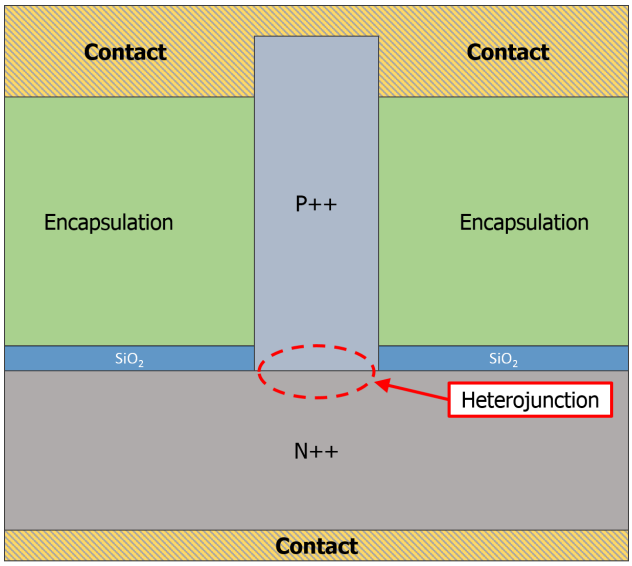
The processing steps after growth are depicted in Figure 5.1 along with a cross-section of a single nanowire in the final structure. In the first step after growth, 450 nm of aluminum was thermally evaporated on the backside of the sample. After evaporation, samples were loaded back into the MOCVD to anneal the contact under arsine for 10 minutes at 500 °C. Annealing under arsine was done to prevent damage to the nanowires from arsenic desorption. Following backside contact anneal, bis-benzocyclobutene (BCB) resin was spin-coated on the samples and hard cured to full polymerization on a 275 °C hotplate for 2 hours in a nitrogen glovebox. After curing, the BCB layer was etched back to expose the tips of the nanowires in a CF_4 / O_2 plasma. Profilometry was used to determine the initial thickness of the BCB layer and calibrate etch rates. Finally, 200 nm thick Ti/Au top contacts were deposited using an electron-beam evaporator. Individual top contacts for each device were created on the sample using a carefully aligned shadow mask. Openings in the shadow mask were the same size as the underlying oxide mesas, 400 μm $\times$ 400 μm. Electrical measurements were made with a Keithley model 4200-SCS parameter analyzer.

5.3 Results and Discussion

Electrical measurements of a GaAs:C / Si:As diode are presented in Figure 5.2. The carbon doped diode array showed a good rectifying characteristic with a forward voltage of approximately 1.1 V, reverse saturation current of 100 pA, and ideality factor of 2.8. Flat regions at the ends of the curve are due to the compliance current of the measurement setup being reached. In this case, compliance was set to 500 μA. Reverse breakdown is observed ranging from -6.0 V to -8.0 V, likely due to Zener breakdown instead of avalanche breakdown due to the low voltage at which it occurred; avalanche breakdown typically only occurs above 10 V bias. In this device, the reverse breakdown voltage monotonically increased with each subsequent measure-



(a)



(b)

Figure 5.1: (a) Process flow for fabrication of a heterojunction diode array. i) Highly doped n-type silicon is used for the substrate, an SAE-NW growth mask is patterned on top. ii) Highly doped p-type GaAs SAE-NWs are grown. iii) After growth, a back contact of thermally evaporated aluminum is deposited and annealed under arsine. iv) The diode array is embedded in an encapsulant which is then hard cured. v) The encapsulant is dry etched in a freon/oxygen plasma, thinning the layer to expose the tops of the nanowires. vi) Top contacts of electron-beam evaporated Ti/Au are deposited using a shadow mask to define individual device contacts for each nanowire array on the sample. (b) A cross-sectional view of a single SAE-NW in the tunnel diode array.

ment. Enhancement effects due to the selective area growth likely lead to a distribution of doping levels among the nanowires and therefore a distribution of Zener breakdown voltages. It is possible that for each measurement, a small number of wires are carrying the majority of the current due to their lower Zener breakdown voltage. Those wires would in turn see more heating and be damaged, leaving the wires with the next lowest breakdown to carry the current in the next sweep. In this way, sets of wires with similar breakdown voltages are successively damaged, explaining the trend observed. Further support for this explanation comes from the fact that after the tenth sweep of the device, it was severely damaged around 3.25 V, evidenced by the sharp drop in current from compliance. This may denote the point at which the last good wires were damaged, and subsequent sweeps show a non-functional device. One such post-destruction sweep is plotted and shows the device no longer rectifies.

Electrical measurements of a GaAs:Zn / Si:As diode are presented in Figure 5.3. The zinc doped diode array showed a good rectifying characteristic with a forward voltage of approximately 1.0 V, reverse saturation current of 16 nA, and ideality factor of 3.9. Reverse breakdown is observed that varied from -3.5 V to -4.1 V. As with the carbon-doped diodes, the Zener breakdown voltage increased monotonically with each successive sweep of the device while the forward characteristic remained nearly identical. Interestingly, the differential in Zener breakdown voltage from sweep to sweep decreased until the breakdown voltage stabilized at its final value. This effect can be reconciled with the polydispersion of doping from a statistical standpoint. Since there is a distribution of nanowire sizes centered around the target diameter, there is likely a majority of nanowires with breakdown voltages near the final value of -4.1 V and decreasing numbers of nanowires with breakdown voltages above and below that. This smaller population of wires with outlying breakdown voltages is more quickly destroyed in the first few sweeps due to their lesser numbers, and as the population of all nanowires is thinned of these outliers, a larger and larger number of wires is present at each successive step in breakdown voltage, explaining the decreasing differential in breakdown change in time. This may indicate that uniformity of the nanowires in the array is even more important than already identified for reasons of current matching, and future devices may even require a sort of 'burn-in' procedure to intentionally remove outlier nanowires.

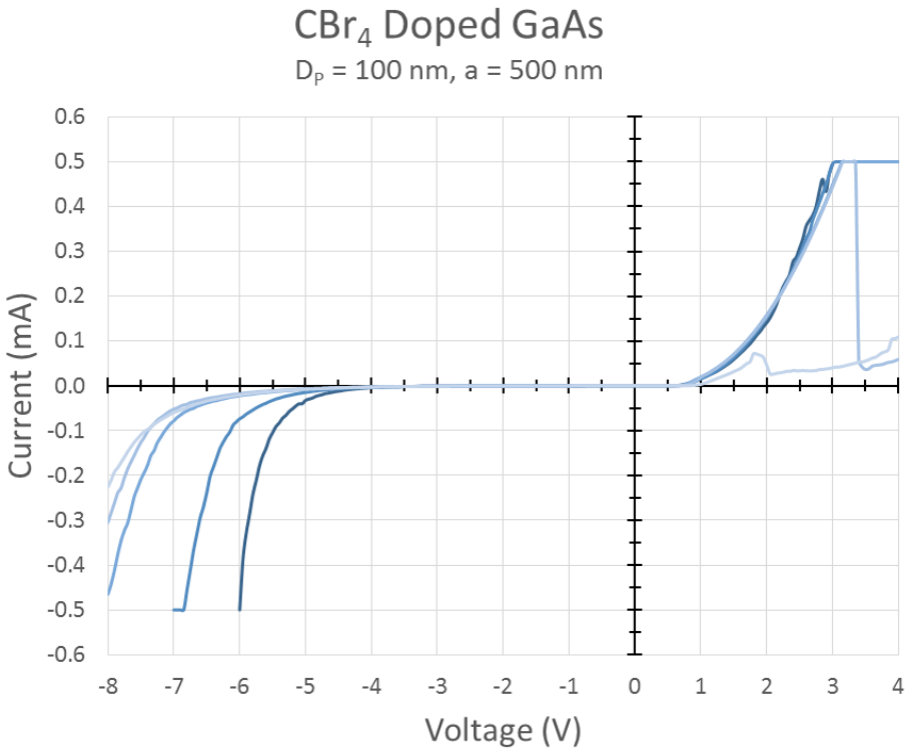


Figure 5.2: Plot of the IV characteristic of one of the GaAs:C / Si:As diodes fabricated in this study. This diode was composed of approximately 40,000 nanowires with D_P = 100 nm and a = 500 nm. Subsequent measurements in time are denoted by decreasing color tint; the darkest trace is the first in time and the lightest is last. As subsequent measurements of this diode were made, the Zener breakdown voltage in the reverse bias drifted monotonically higher, while the forward characteristic remained unchanged. After the tenth sweep of the device, it was damaged around 3.25 V. In subsequent sweeps, the device is non-functional as it is no longer rectifies. One example sweep post-destruction is plotted (lightest in color).

Although this device was never completely destroyed, the forward characteristic did noticeably droop in the last three sweeps, indicating an increase in the resistance in the device, likely from damage. This is consistent with the idea that there is polydispersion in Zener breakdown voltage of individual nanowires, which was used to explain the monotonic drift in reverse breakdown. Whereas doping level strongly influences Zener breakdown voltage, the forward characteristic of a diode is more strongly influenced by the band gap of the material, which determines the point to which the junction needs to be biased for current to flow. Therefore, the nanowires will conduct the forward current more evenly than the reverse current. However, as more and more nanowires are destroyed due to damage during reverse bias, the current carrying capacity of the diode is reduced eventually showing a droop in the forward characteristic due to an effective increase in the series resistance of the device.

Band diagrams for the structure fabricated in this study are plotted in Figure 5.4, separately for silicon substrate doping of 5.0 mΩ-cm and 2.0 mΩ-cm to serve as a high and low case for the lot of substrates used. Since dopant incorporation into SAE-NWs is not well studied or understood, it is not possible to predict the exact doping level in the wires. Due to this, in each band diagram several p-type doping levels for the GaAs are plotted to represent a range of likely possibilities. Although an imprecise method, doping level can be estimated from the band diagram with knowledge of the Zener breakdown voltage. For Zener breakdown to occur the junction must be biased to the point where band bending has caused the spacing at the Fermi level between the valence and conduction bands to narrow to the point at which quantum tunneling can occur (∼10 nm). Using this method, it can be estimated that the p-type doping in the diodes fabricated in this study is significantly below 1.0×10^{19} cm^{-3}. In addition to increasing the p-type doping to achieve a tunnel diode, the n-type doping could also be increased. The band diagram for fixed p-type doping for several levels of n-type doping is plotted in Figure 5.5. It can be seen that pushing silicon doping past the mid-nineteenth order of magnitude cm^{-3} has negligible effect on the junction, especially compared to the effect of increasing the doping in the III-V nanowire past the same level.

Here, fabrication and measurement of heterojunction diodes by using the SAE-NW technique to grow GaAs on silicon substrates has been presented.

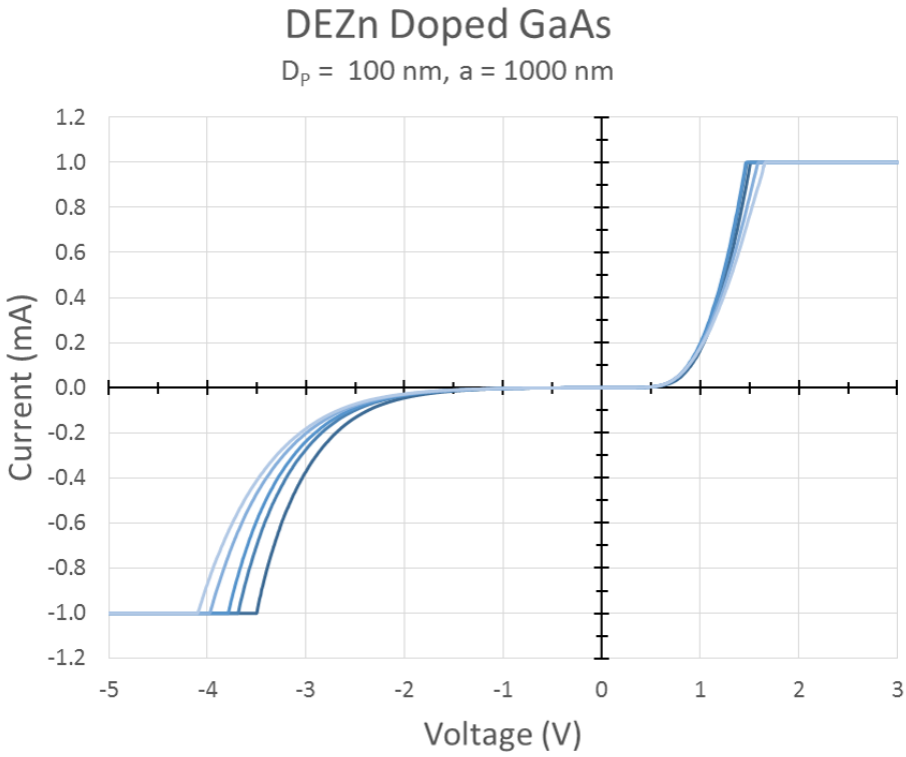
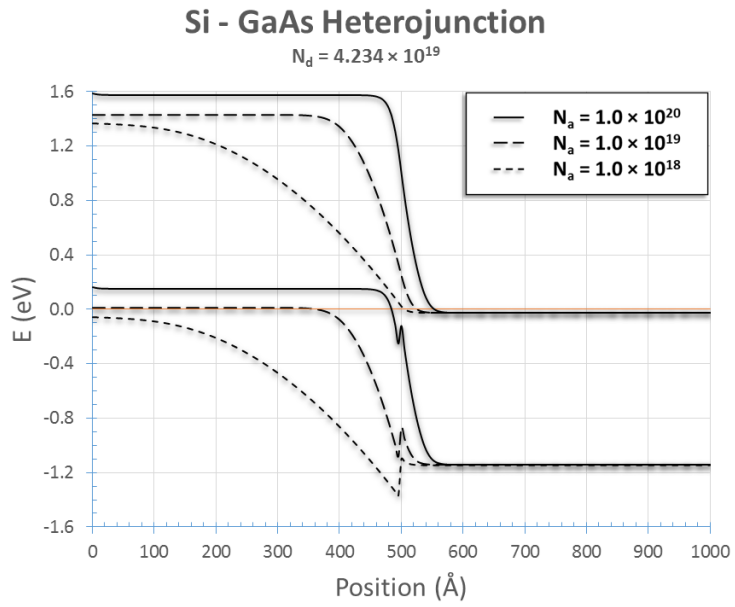


Figure 5.3: Plot of the IV characteristic of one of the GaAs:Zn / Si:As diodes fabricated in this study. This diode was composed of approximately 10,000 nanowires with D_P = 100 nm and a = 1000 nm. Subsequent measurements in time are denoted by decreasing color tint; the darkest trace is the first in time and the lightest is last. As subsequent measurements of this diode were made, the Zener breakdown voltage in the reverse bias drifted monotonically higher; however, in contrast to the carbon doped diode, the forward characteristic began to droop on the last sweeps of the device indicating an increase in resistance, likely from damage.



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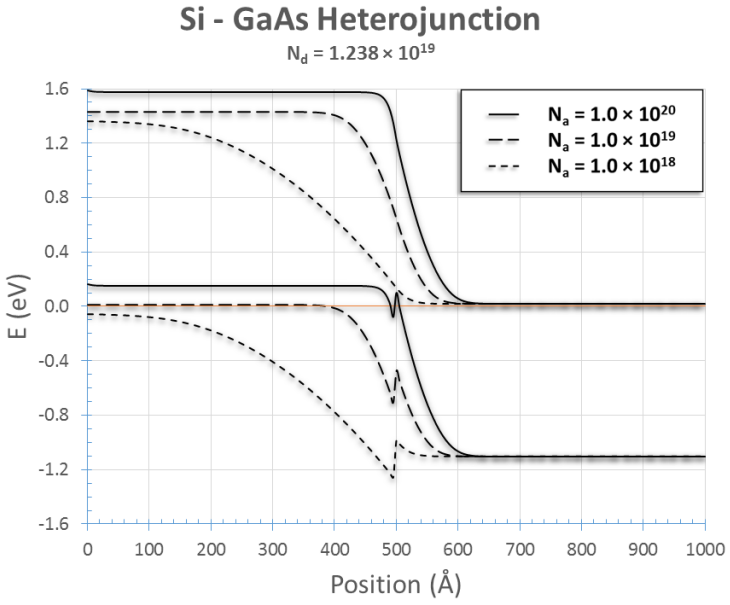


(b)

Figure 5.4: Band diagram for a GaAs - Si heterojunction. Silicon doping level varies according to the maximum and minimum resistivity range specified for the wafer lot used in this experiment of 2.0 to 5.0 mΩ-cm. (a) $R_{Si:As}$ = 5.0 mΩ-cm, (b) $R_{Si:As}$ = 2.0 mΩ-cm.

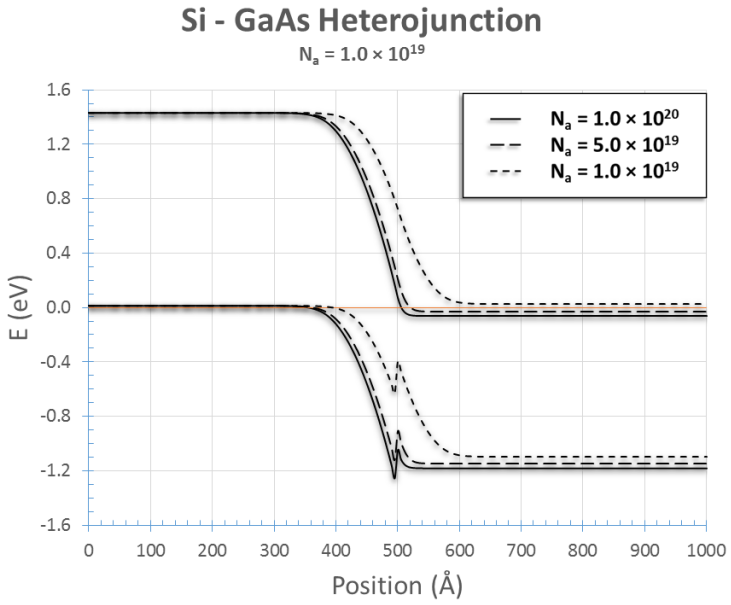


Figure 5.5: Band diagram for a GaAs - Si heterojunction. GaAs doping level is fixed at $N_a = 1.0 \times 10^{19}$ cm^{-3} and silicon doping varies over three orders of magnitude. Note the minimal effect as silicon doping is increased into the twentieth order of magnitude cm^{-3}.

These experiments elucidate a path to realization of a tunnel junction for tandem nanowire-on-silicon solar cells. A trend has been identified in which the Zener breakdown voltage of these diode arrays decreases monotonically with stress, likely due to polydispersion in doping in the nanowires caused by selective enhancement effects on the dopant species during growth. This effect indicates that uniformity in the array is critical to achieving a device with stable properties in time, without a burn-in process. Although further study and optimization are required to achieve a tunnel diode, a path to that device has been shown.

CHAPTER 6

FUTURE DIRECTIONS

The results presented in Chapters 4 and 5 represent only a small fraction of the experiments that have been discussed and carried out during the course of this work to study the selective area epitaxy technique. Many experiments hinted at effects that have yet to be adequately characterized. In this chapter, future directions for the continuation of this work will be presented. These topics are at various stages of maturity; some include initial experiments whereas others are simply thoughts that have yet to be fully formed.

6.1 Systematic Doping Study

New growth techniques that depart from conventional epitaxy such as VLS and SAE show great promise for use in next-generation devices. With these techniques, it is possible to build devices with a bottom-up approach enabling new possibilities and possibly lowering cost through reduction in processing steps. However, fundamental differences in these growth techniques could modulate doping through a number of effects including: preferential incorporation of dopants on a particular crystal plane when multiple facets are present on a three-dimensional growth front, differential adsorption of a dopant into a VLS catalyst, and differential enhancement rates for dopant and growth precursors in SAE. Controllable doping of material, both p-type and n-type, over a range of several orders of magnitude is critical to designing useful and efficient semiconductor devices. As such, a thorough understanding of doping in the SAE-NW technique and its departures from traditional planar epitaxy of III-V materials is necessary for realization of viable devices. To date, doping has been done by tailoring growth conditions such that equivalent planar growth would be degenerate; however, the underlying doping mechanism is still not well characterized or in some cases even

completely understood. A better understanding of doping in SAE-NWs is critical to advancement of the field.

6.1.1 Zinc Dopant Diffusion Study

It has been known for decades that although zinc is a fantastic p-type dopant in GaAs capable of achieving very high doping levels, it also is handicapped by its high diffusion [77]. This fact complicates structure growth as zinc layers must be incorporated with a thermal diffusion budget in mind. The end result is that zinc is typically only useful for p-on-n type structures where the p-type layer is on top of the structure and therefore grown last, minimizing the amount of time the zinc containing layer is at high temperature and susceptible to high diffusion rates. It is impractical to grow a highly zinc-doped layer beneath a thick epitaxial structure such as would be necessary for an n-on-p device.

For the growth of zinc-doped GaAs SAE-NWs, this diffusion is especially concerning due to the typically low growth rates used and high growth temperatures as discussed in Section 2.3. In this work, zinc-doped GaAs SAE-NWs have been successfully grown with good morphology. To limit zinc diffusion, growth rates faster than in typical SAE-NW conditions have been investigated by increasing Group III precursor flow up to 3.3×. This faster growth rate has a two-fold effect of both reducing time at high temperature and also possibly increasing zinc incorporation, which is a well-known effect in conventional planar epitaxy [78]. Initial results show that nanowires grown at this higher rate exhibit good morphology as shown in Figure 6.1. Future investigation could focus on confirmation and quantification of a zinc incorporation dependence on growth rate, as exists in conventional planar epitaxy. As with all dopants, efforts could also be directed towards quantification of the doping level via resistivity measurements using advanced nanowire measurement like the micro-four-point probe technique [79, 80, 81].

6.1.2 Silicon Surfactant Effect Study

Silicon is a commonly used n-type dopant during growth of GaAs with disilane (Si_2H_6) commonly used as a precursor [82]. In this work, we have

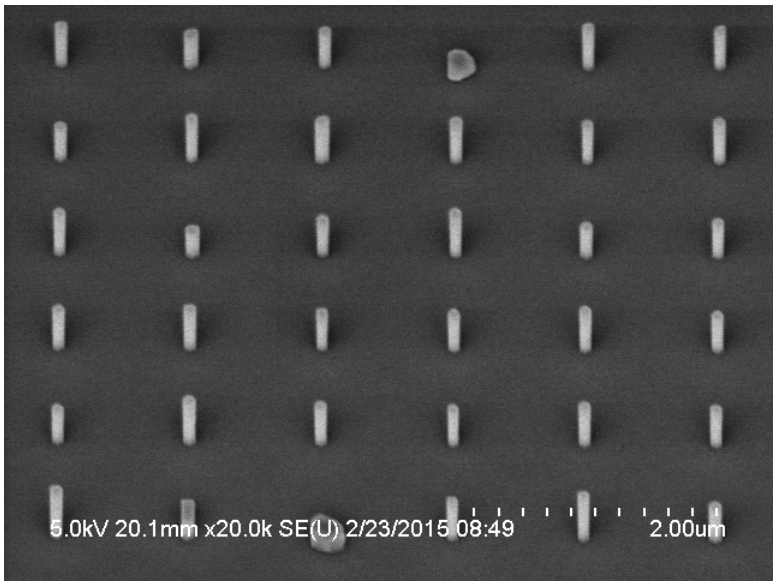


Figure 6.1: Zinc-doped GaAs SAE-NWs grown with 3.3× the typical Group III precursor flow. No detrimental effect on morphology was observed. These particular nanowires are grown on (111) oriented silicon substrates.

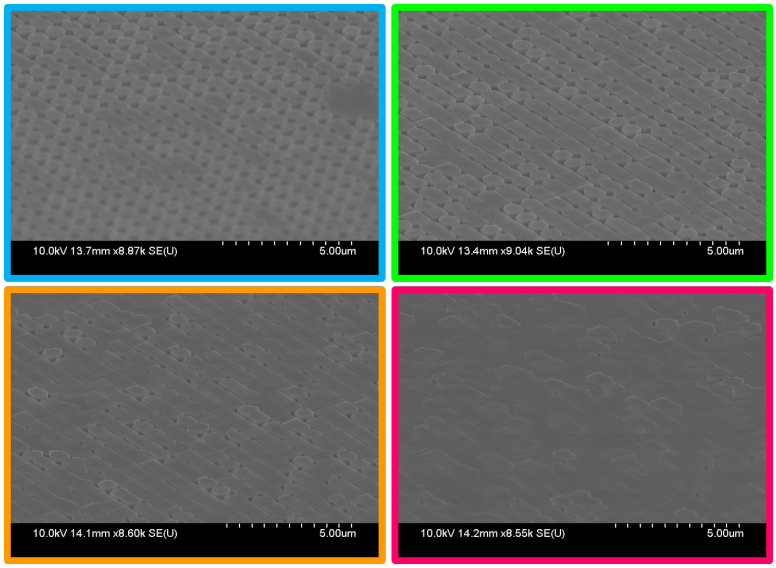
observed that silicon doping of GaAs SAE-NWs using Si_2H_6 detrimentally modulates the SAE-NW growth mechanism, which has already been reported in another study [83]. Figure 6.2 depicts the results of an Si_2H_6 doping experiment in which the lateral growth rate was significantly enhanced compared to a similar growth with no Si_2H_6 flow. In this experiment, the entire array of SAE-NWs eventually coalesced together into one large island. A gradation of this effect could be observed moving from the edge of the array towards the middle, providing evidence that this effect might scale with enhancement level. Due to the larger growth enhancement toward the edge of the array, the wires coalesced completely. In the middle of the array where the enhancement would be slightly less, the wires had grown radially quite close, but had not yet completely coalesced. Figure 6.3 shows a view of the corner of the GaAs:Si SAE-NW array where the nanowires are completely coalesced. This morphology is in stark contrast to that seen when disilane is not introduced during growth. It is hypothesized that the silicon may have a surfactant effect on the {110} sidewalls of the nanowires leading to a breakdown of the typically high growth rate asymmetry between the (111) end facet and {111} sidewalls discussed in Section 2.3. Future investigation

could focus on this possible surfactant effect and explore the growth parameter space in search of conditions for which this effect is suppressed. As with all dopants, efforts could also be directed towards quantification of the doping level via resistivity measurements using advanced nanowire measurement like the micro-four-point probe technique [79, 80, 81].

6.1.3 Group IV Dopant Amphoterism Study

Group IV dopants such as carbon and silicon are commonly used in III-V materials. For typical planar epitaxy on common (100) substrates it is well known that carbon preferentially incorporates on Group V sites as a p-type dopant, whereas silicon preferentially incorporates on Group III sites as an n-type dopant. Unfortunately for the SAE-NW technique, this incorporation dependence does not necessarily hold due to the use of a (111) oriented substrate because Group IV elements are known to be amphoteric on the {111} planes of III-V materials. However, functional SAE-NW devices based on doping with these elements have been reported indicating that preferential incorporation on either Group III or Group V sites is occurring. Other results have shown that dopants may actually predominantly incorporate on the {110} sidewalls instead of the (111) end facet of the nanowires as discussed in Section 6.1.2. If Group IV dopants are in fact predominantly incorporated on the sidewalls of the nanowire, a gradient in their composition should be observable due to the radial growth inherent to the SAE-NW technique that was discussed in Chapter 4. In the beginning of growth, when the SAE-NW is short, it has a smaller diameter than later when it gets taller. This means that a thicker shell of dopant-containing material should exist at the bottom of the nanowire and a much thinner shell at the top where the core of the nanowire started at a larger diameter and the shell of the dopant-attracting sidewall has been exposed for a shorter time. Effectively, there should be an upside-down cone of intrinsic or compensated material at the core of SAE-NWs doped with Group IV elements. Future efforts could attempt to confirm this through the use of atom probe microscopy [84].

(a)



(b)

Figure 6.2: (a) A diagram of an SAE-NW array experiment depicting the areas in which various levels of silicon-induced growth modulation occurred. Nanowire arrays are defined by a PECVD deposited silicon dioxide growth mask. A (111)B oriented GaAs substrate was used in this experiment. The four colored areas show the areas where varying degrees of coalescence were observed, likely due to differences in local partial pressure from enhancement effects. (b) SEM images showing areas of varying coalescence corresponding to the colored areas depicted in (a).

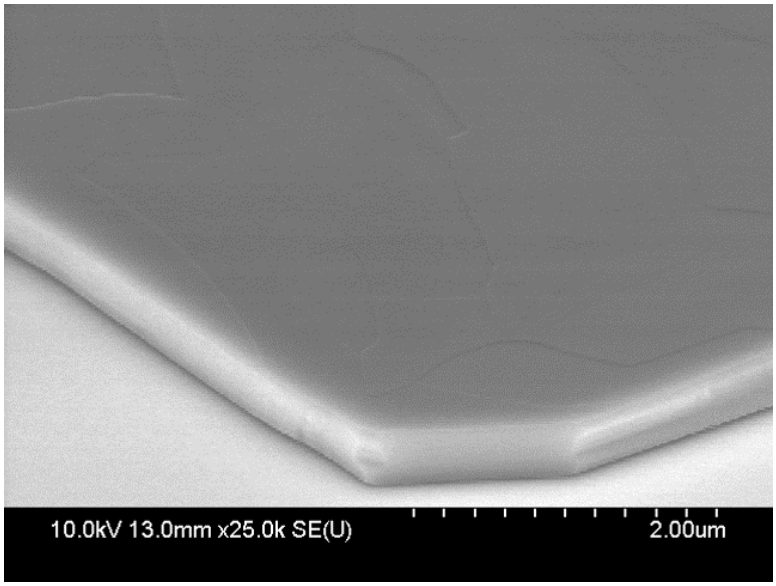


Figure 6.3: SEM image of the corner of the same SAENW array from Figure 6.2 which was doped heavily with silicon using Si_2H_6. In this area you can more clearly see the nanowires have coalesced together into a solid island.

6.1.4 Halide Dopant Etch-back Study

In the GaAs material system, zinc exhibits high diffusion and can only be used in the top layers of an epitaxial structure, as discussed in Section 6.1.1. For internal p-type layers such as upper laser cores, a dopant that does not diffuse as readily is needed. Carbon is often used and can be incorporated in a number of ways. At low III-V ratio, carbon can be incorporated intrinsically from methyl groups shed by metal-organic precursors and adsorbed onto the surface. For high carbon doping, though, it is necessary to use a carbon precursor, commonly the halides CBr_4 and CCl_4. Halogens are commonly known to etch III-V materials, and the halogen content of these precursors can lead to etching of the III-V material as it grows. This effect is known as etch-back [85]. In this work, GaAs SAE-NWs doped using CBr_4 have been grown. The growth rates of these wires were reduced compared to undoped wires as expected, likely due to etch-back, but the morphology of the wires was good and no significant modulation of the crystal plane dependent growth rate asymmetry central to the SAE-NW technique was observed, as can be seen in Figure 6.4. Interestingly, preliminary measurements point

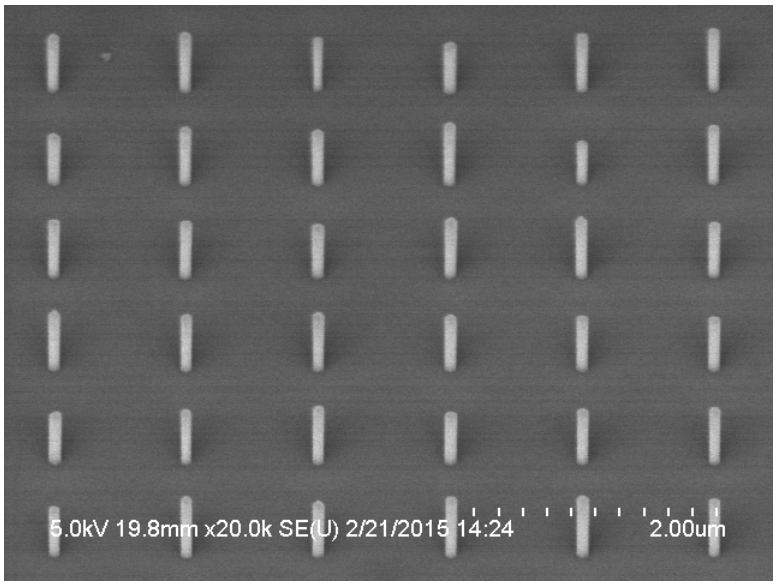


Figure 6.4: Carbon-doped GaAs SAE-NWs grown using as CBr_4 a precursor. These nanowires exhibited good morphology, but initial growths do indicate a reduction in the growth rate due to well-known etch-back effects. More interestingly, the etch-back seems possibly to be modulated by enhancement effects. These particular nanowires are grown on (111) oriented silicon substrates.

to selective area enhancement of etch-back effects. Larger spacing between nanowires typically results in higher growth rates due to enhancement effects, as discussed at length in Chapter 4. Initial indications are that this trend does not hold when CBr_4 is introduced during growth. In the latest experiment, the nanowires with the lowest array density and therefore the highest enhancement were actually the shortest on the sample. This points to the possibility that the etch-back rate is increasing through enhancement of the halide partial pressure. Future efforts could focus on performing a more detailed statistical analysis of large nanowire arrays to confirm the existence of this effect and exploration of a wider parameter space which may reveal a quantifiable trend for this effect.

6.2 Porous Masks

Lithography, especially electron-beam lithography, is expensive. Promising device designs are often limited by the infeasibility of scaling for production. Many nanotechnology techniques seek to overcome this limitation by leveraging serendipitous natural self-assembly phenomena to easily fabricate structures that in the past would have been cost-prohibitive, or physically impossible to produce. In this way, expensive lithography processing steps can be minimized having been replaced by nanotechnology based methods.

In this work it has been observed that, with an appropriate surface treatment, it is possible to create a self-assembled mask for SAE-NW growth, bypassing the need for any lithography steps. Figure 6.5 shows an experiment in which an EBL patterned sample was unintentionally over-etched during surface preparation for growth. Oxide deposited via PECVD, as was used on this sample, is notoriously porous compared to thermally grown native oxide on silicon. Compounding the inherent lower quality of the oxide is the damage it sustains during the multiple plasma ashing steps necessary for SAE-NW growth. As a result, the thin oxide layers are susceptible to pinhole formation during wet etching. In Figure 6.5 you can see nine nanowires from intentionally defined EBL patterning in addition to a collection of nanowires that grew out of pinholes in the growth mask in a self-assembled fashion.

Upon discovery of this effect, a larger scale experiment was carried out to see if a reasonable amount of control and uniformity could be achieved over a wide area. Figure 6.6 shows the result of this experiment. The sample showed a high density of self-assembled SAE-NWs with surprisingly good uniformity. Although high degrees of order in the nanowire arrays are necessary for some applications like photonic crystals or where integration of single wires is desired, these types of random arrays can be used for light-emitting devices to improve extraction efficiency or solar cells to improve light absorption. A major issue identified with this technique has been the narrow process window over which the effect yields good results; results varied significantly over the surface of samples. Future work could focus on expanding on the limited number of experiments that have been carried out to seek a window in which the process is more repeatable and forms more uniform arrays. Dilution of the 50:1 buffered oxide etchant has been proposed as a starting point to increase the etch times and widen the process window.

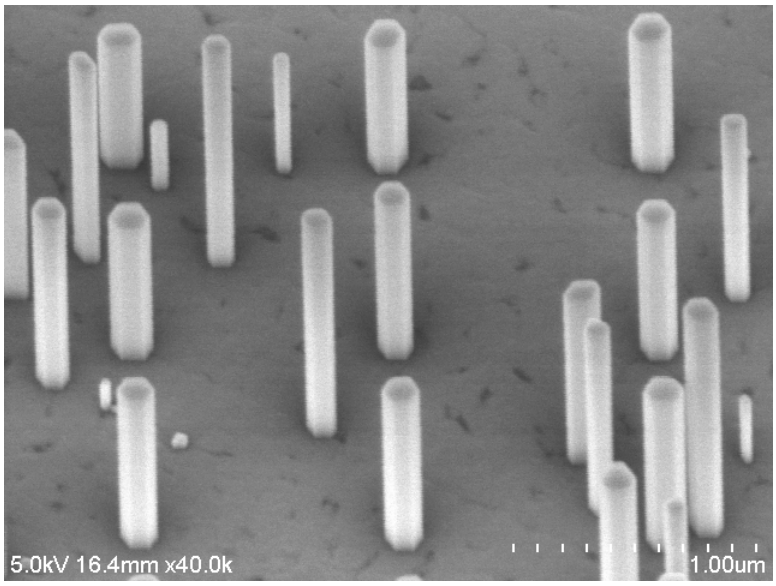
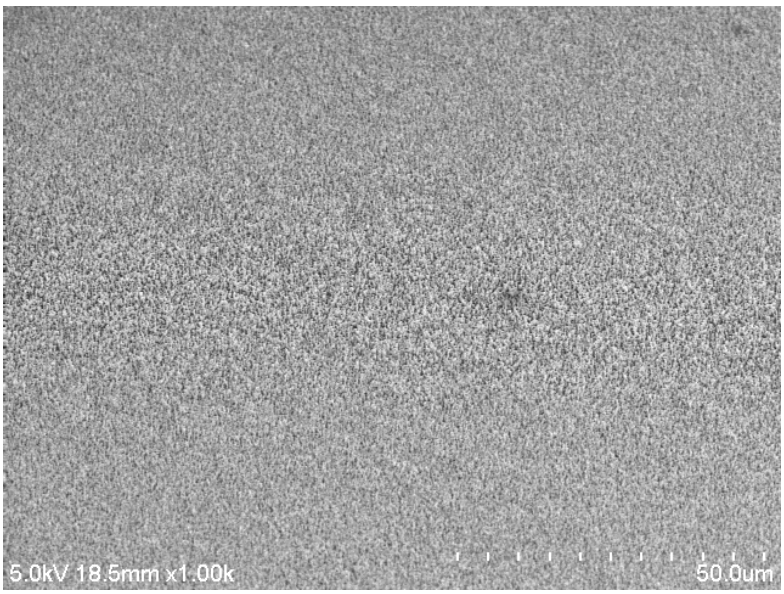


Figure 6.5: An electron-beam patterned wire array is present along with wires that formed due to pinhole defects in the oxide caused by over-etching. Note that nine of the wires are spaced in a precise 1 μm square lattice; these are part of the intended lithographically defined array.

6.3 Suspended Waveguides

Photonic crystal structures based on SAE-NWs were discussed in Section 3.5. A major limitation of those demonstrations was the necessity to remove the SAE-NW structure from its growth substrate to provide out-of-plane optical confinement. This significantly degrades performance of devices due to the poor thermal characteristics of a structure embedded in polymer suspended in air and makes contacting the device electrically very difficult, thus limiting the prospects for electrically injected devices. Due to the inability to effectively remove heat from a nanowire structure removed from its substrate, lasers would need to be operated at low powers and in pulsed mode to prevent destruction of the device. If a thermal connection to the substrate could be maintained while achieving out-of-plane optical confinement, a photonic crystal laser with significantly improved performance could be demonstrated. Furthermore, growth on a silicon substrate instead of GaAs could result in even better thermal characteristics due to the higher thermal conductivity of silicon.

A suspended waveguide structure could improve out-of-plane optical con-



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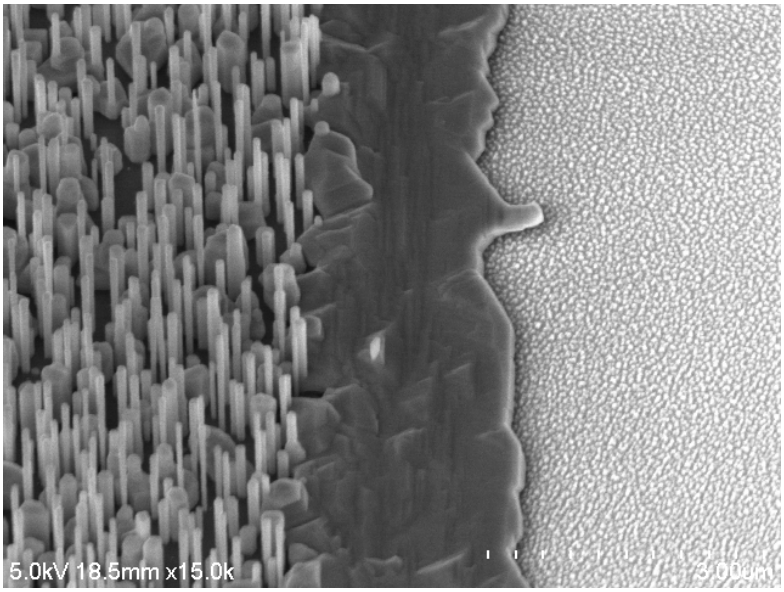


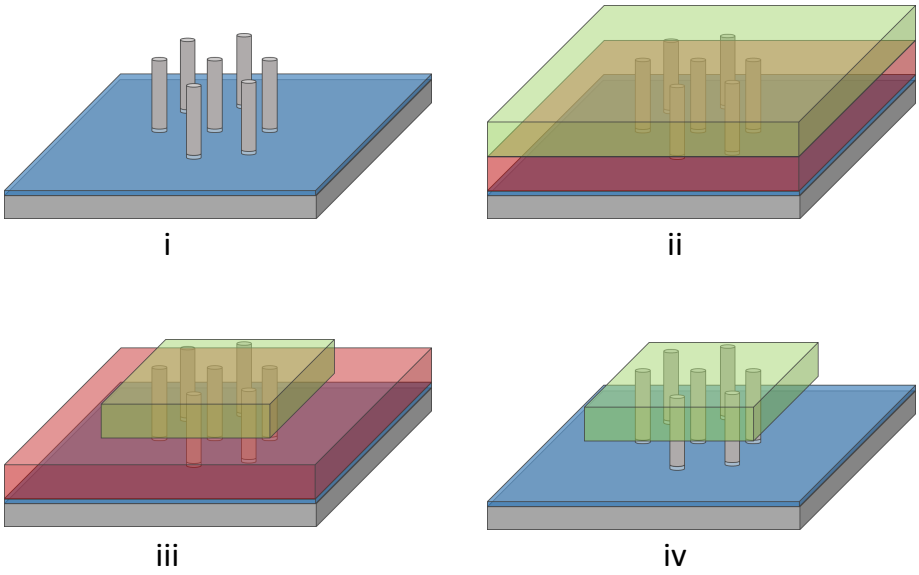
(b)

Figure 6.6: (a) A wide area view showing the uniformity of wires grown using the porous mask technique on silicon. (b) A region on the border of the porous mask and a thick oxide mask. Note the lack of growth on the thick oxide mask and the bulk-like growth in the border region due to the extreme enhancement due to the location next to a large oxide patch.

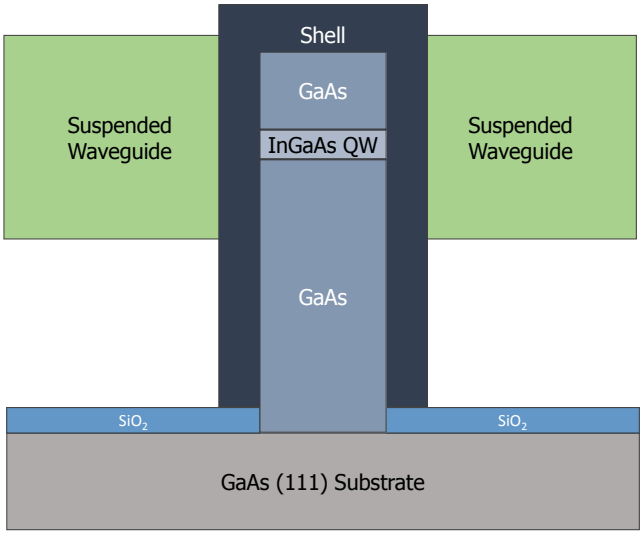
finement in SAE-NW photonic crystal structures while keeping a thermal and electrical connection to the growth substrate. Figure 6.7 depicts an example process for such a device. In this structure the air-gap between the dielectric photonic crystal layer and the substrate acts as a slab waveguide, reducing guiding of the optical mode into the substrate. Finite-difference time-domain (FDTD) simulation could be used to design and evaluate the effectiveness of this method before time-consuming fabrication is attempted. A number of bilayer combinations could be envisioned to fabricate such a structure, although a UV cured polymer encapsulant on top of photoresist is perhaps the most promising. Other combinations involving BCB, SU-8, SOG, etc., could also be envisioned although careful attention would need to be paid as some of these materials require extended cure times at moderate to high temperature which could have detrimental effects on the spacing layer. Future efforts should focus on first verifying with FDTD analysis the geometry needed to realize beneficial optical confinement before developing a robust process for creating suspended layers in the nanowire array.

6.4 Tandem Nanowire-on-Silicon Solar Cell

As discussed in Section 3.4, theoretical analysis has shown that the limiting efficiency for a nanowire-on-silicon solar cell is 38.8% [60]. This means it is quite possible a nanowire-on-silicon tandem junction solar cell would be nearly as efficient as state-of-the-art triple and quad junction solar cells while being cost-competitive with common single crystal silicon cells. Future efforts on the development of a tandem nanowire-on-silicon solar cell should focus on continuing the experiments presented in Chapter 5 to develop an effective tunnel diode to connect the sub-cells and lead into process development for a fully functional device. An example process and structure for a hypothetical tandem nanowire-on-silicon solar cell are depicted in Figure 6.8.

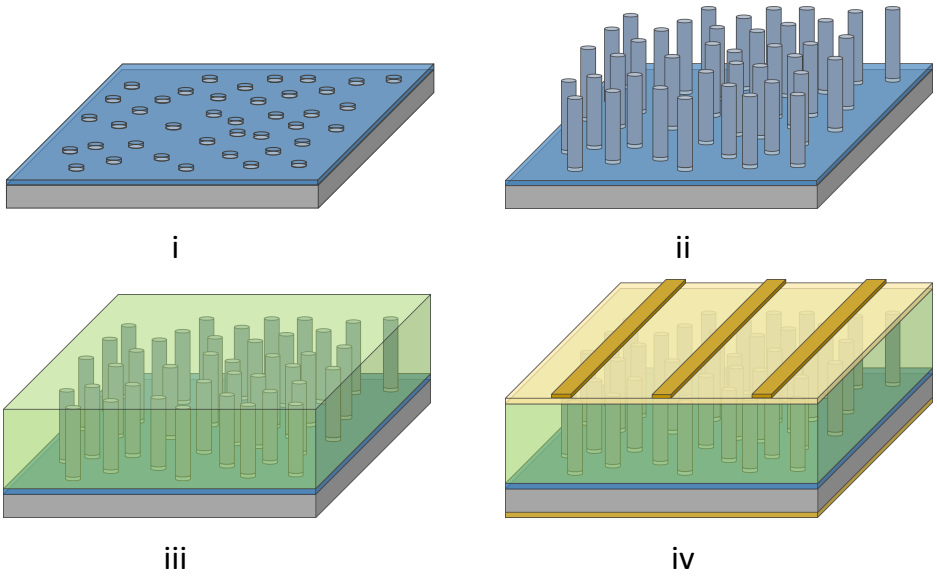


(a)

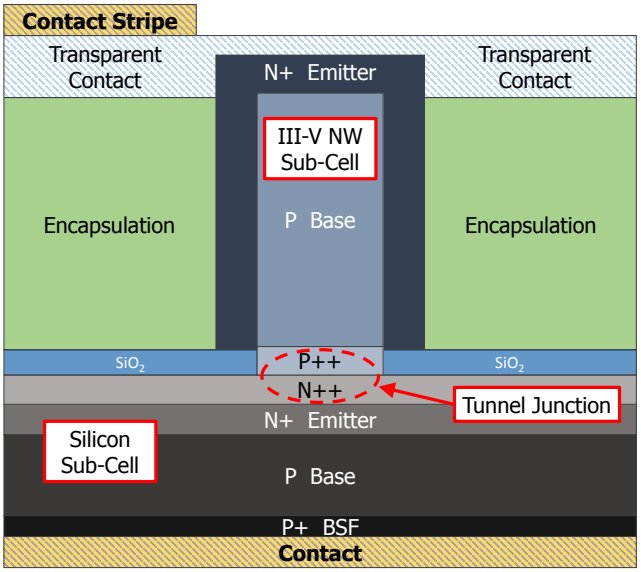


(b)

Figure 6.7: (a) Process flow for fabrication of a suspended waveguide photonic crystal structure. i) A photonic crystal resonator is designed and grown from SAE-NWs. ii) A bilayer of PR and encapsulant is spin-coated on the sample. iii) The waveguide structure is defined via lithography. iv) The PR is removed leaving the waveguide suspended. (b) A cross-sectional view of a single SAENW in the photonic crystal array showing the location of the InGaAs quantum well in relation to the suspended waveguide.



(a)



(b)

Figure 6.8: (a) Process flow for fabrication of a tandem junction nanowire solar cell. i) A silicon p-n junction lower cell is used for the substrate, an SAE-NW growth mask is patterned on top. ii) A thin tunnel diode layer is grown followed by a radial core-shell junction GaAs top solar cell. iii) The tandem structure is embedded in an encapsulant. iv) Top and bottom contacts are deposited for electrical connections. A stripe array combined with a transparent conductor layer such as ITO or graphene is used for the top contact to allow light into the cell. (b) A cross-sectional view of a single SAE-NW in the tandem junction array.

CHAPTER 7

CONCLUSION

Selective area epitaxy of nanowires is a promising technique for the growth of high quality III-V nanostructures for use in next-generation devices. Nanowires grown via the SAE technique exhibit many advantages over other commonly studied growth mechanisms such as VLS. The use of a growth mask makes SAE-NWs inherently patternable, and both dimension and location are easily controlled. The lack of a seed particle improves the quality of growth by eliminating the incorporation of trace impurities into the semiconductor material, and the high temperature MOCVD growth produces high quality crystals with nearly atomically flat facets and untapered sidewalls.

In this thesis, after a brief introduction to the key techniques that build upon each other to form the SAE-NW process, the state of the art in the field was reviewed. Reports on SAE-NW devices such as light emitters, sensors, and devices for solar energy conversion were discussed. Following that, a detailed study of the evolution of nanowires during growth was presented which established geometry-induced limiting effects during the growth of GaAs SAE-NWs. This study quantified the breakdown of hexagonal symmetry in SAE-NWs due to these geometry-induced effects and established guidance for growth of perfect nanowire arrays for devices. Experiments and results were then presented on the path to development of a tunnel diode for a nanowire-on-silicon tandem junction solar cell. Finally, future directions for the study of the SAE-NW technique were outlined with preliminary results in some areas. Proposed studies focused on furthering the understanding of doping mechanisms in SAE-NW growth and quantifying the doping effects, an essential step towards the realization of high quality commercially viable devices.

There is much active ongoing research in the field of selective area epitaxy grown nanowires, and there is much yet to do. As a truly commercially viable technique with a direct and demonstrated path to integration on silicon sub-

strates, SAE-NWs merit research effort and further investigation will likely uncover unimagined possibilities.

APPENDIX A

EPITAXIAL GROWTH OF THREE-DIMENSIONALLY ARCHITECTURED OPTOELECTRONIC DEVICES

Optoelectronic devices have long benefited from structuring in multiple dimensions on microscopic length scales. However, preserving crystal epitaxy, a general necessity for good optoelectronic properties, while imparting a complex three-dimensional structure remains a significant challenge. Three-dimensional (3D) photonic crystals are one class of materials where epitaxy of 3D structures would enable new functionalities. Many 3D photonic crystal devices have been proposed, including zero-threshold lasers [86, 87], low-loss waveguides [88, 89, 90], high-efficiency light-emitting diodes (LEDs) and solar cells [91, 92, 93], but have generally not been realized because of material limitations. Exciting concepts in metamaterials, including negative refraction and cloaking, could be made practical using 3D structures that incorporate electrically pumped gain elements to balance the inherent optical loss of such devices [94]. Here we demonstrate the 3D-template-directed epitaxy of Group III-V materials, which enables formation of 3D structured optoelectronic devices. We illustrate the power of this technique by fabricating an electrically driven 3D photonic crystal LED.

This appendix is reprinted with permission from E. C. Nelson, N. L. Dias, K. P. Bassett, S. N. Dunham, V. Verma, M. Miyake, P. Wiltzius, J. A. Rogers, J. J. Coleman, X. Li, and P. V. Braun "Epitaxial growth of three-dimensionally architectured optoelectronic devices," *Nature Materials*, vol. 10, p. 676-681, Jul 2011. ©2011 Macmillan Publishers Limited. [http://doi.org/10.1038/nmat3071]. We would like to thank M. Sardella and J. Soares of the Materials Research Lab for experimental assistance and helpful discussions. The 3D epitaxy growth process development was supported by the US Army Research Office Award #DAAD19-03-1-0227, fabrication and testing of optoelectronic devices was supported by the US Department of Energy 'Light-Material Interactions in Energy Conversion' Energy Frontier Research Center Award #DE-SC0001293, design of optoelectronic devices was supported by the US Department of Energy 'Center for Energy Nanoscience' Energy Frontier Research Center Award #DE-SC0001013, and optimization of the MOCVD reactor was supported by NSF Award #0749028.

A.1 Introduction

Despite significant efforts over the past two decades, the development of 3D structured materials that possess the requisite low defect density for optoelectronic functionality has remained elusive. There are many pathways by which to impart a complex 3D structure into amorphous or polycrystalline materials [95, 96, 97, 98], however such materials have poor electrical properties. In particular, for optoelectronic devices where long carrier lifetimes are required, it will almost certainly be necessary to form the 3D structure from a single-crystal, direct-bandgap semiconductor to minimize undesired recombination and other losses. Approaches based on the patterning of single-crystal starting materials, including anisotropic dry etching [99], wafer bonding [100] and layer-by-layer [101, 102] assembly techniques, are intriguing. However, they are limited to specific 3D structures and materials, and often contain undesirable defects; thus, as far as we are aware, optoelectronic activity has not been demonstrated so far from any device formed using these approaches.

Here we demonstrate the epitaxial growth of Group III-V semiconductor 3D nanostructured materials, including those containing light-emitting heterostructures, by selective area epitaxy (SAE) through a 3D template. As traditionally performed, selective area epitaxy is a process during which a two-dimensional (2D), typically oxide, mask is patterned on a semiconductor wafer and material is subsequently grown by metal-organic chemical vapor deposition (MOCVD). Growth occurs only on the exposed regions of semiconductor, resulting in a patterned film. We show that a 3D nanostructured mask can be used in conjunction with MOCVD to epitaxially grow a 3D structured, optoelectronically active, GaAs-based material—in this case, a 3D photonic crystal. Epitaxy is preserved even as the GaAs grows through the complex geometry of the template.

A.2 Results and Discussion

A representative 3D photonic crystal is shown schematically and in the scanning electron microscope (SEM) cross-section image in Figure A.1(a). The SEM image shows a colloidal crystal template that has been partially filled from the substrate upwards with GaAs by means of selective area epitaxy.

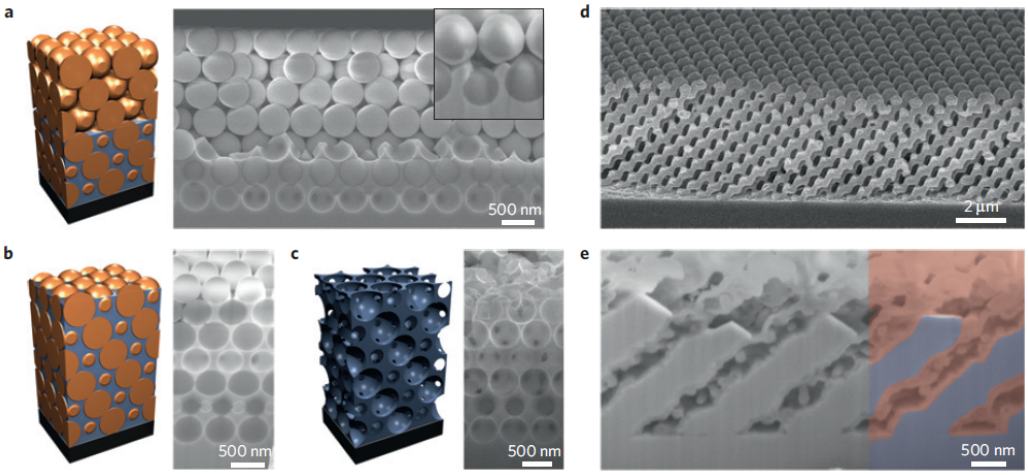


Figure A.1: Three-dimensionally patterned GaAs photonic crystals. (a) Schematic and SEM of a 3D photonic crystal template partially filled with GaAs by epitaxy. Inset highlights off-normal growth directions that occur when the GaAs grows around the template. Schematic and focused ion-beam cross-section SEM images of (b), GaAs filled template and (c), inverted (template removed) GaAs structure. (d) Polymer template formed by multibeam interference lithography. The template was filled with alumina and the polymer was removed, providing a template with high temperature stability for GaAs growth. (e) The GaAs filled the alumina template. GaAs is shown in blue and alumina in red in the colorized image.

Growth initiates in the [001] direction from the GaAs (001) wafer surface, however to grow around the template the growth front propagates in various directions. This is observed in the inset of Figure A.1(a), where the growth front moves off-normal to propagate around the template. After the template is almost completely filled (Figure A.1(b)), it is etched, leaving a porous 3D semiconductor structure (Figure A.1(c)). We intentionally underfill the template to prevent formation of a sealed surface, which would lead to difficulty removing the template. Three-dimensional SAE was also performed through polymer templates created using interference lithography by first converting the template to a thermally stable material such as alumina (Figure A.1(d)), followed by growth of GaAs and removal of the template (Figure A.1(e)), providing a route to almost any 3D structure, given the versatility of interference lithography [98, 103, 104].

The fact that the growth begins at the substrate, and proceeds upwards, is only evidence of selective area deposition, not epitaxy. Epitaxy of the

photonic crystals was quantitatively confirmed using $2\theta/\omega$ X-ray diffraction (Figure A.2(a)), electron diffraction (Figure A.2(c),(d)) and texture measurements (Figure A.2(b)) on samples after template removal (for example Figure A.1(c)). In the $2\theta/\omega$ measurements only the GaAs (002)/(004)/(006) peaks were detected, indicating a common out-of-plane lattice spacing between the photonic crystal and the substrate. The crystalline nature of the deposit (Figure A.2(c)) was confirmed by electron diffraction (Figure A.2(d)). Epitaxy was confirmed by pole figure analysis (Figure A.2(c)), which shows four strong peaks at 45° originating from (220) reflections. The pole figure also shows several additional peaks that are due to (111) twinning in the film, which often occurs during growth of Group III-V nanostructures, such as nanowires.

Traditional 2D selective area epitaxy relies on a strong preference for growth on the semiconductor substrate rather than the mask material [35, 34, 105, 106]. When applied to planar device fabrication, if a small amount of nucleation occurs on the mask surface the nuclei are typically removed when the mask is etched. However, if nucleation occurs on the surface of our 3D masks (Figure A.3(a)) a polycrystalline film will result, because the surface nuclei penetrate downward into the template as shown in Figure A.3(b) and merge with the upward propagating growth front, resulting in incorporation of polycrystalline material into the 3D structure. Elimination of surface nucleation is a critical component for successful 3D SAE. It is known that an interplay between the growth temperature, reactor pressure, and the partial pressures of the Group III precursors controls the rate of heterogeneous nucleation during SAE [33, 107]. Diffusion of the precursors through the 3D template is reduced in comparison with the bulk gas phase, resulting in an increased partial pressure of the source materials over the 3D mask, which affects the heterogeneous nucleation behavior. Therefore, conditions for selective growth are different for 2D and 3D masks and must be elucidated [107].

The rate of heterogeneous nucleation is also strongly influenced by the thickness of the template (for example the number of layers or periods) because this affects the partial pressure of precursor over the template owing to the reduced diffusivity through the 3D structure. The effect of template thickness or diffusion distance on precursor partial pressure is presented in Figure A.3(c)-(e), where the nucleation density is high, moderate and ap-

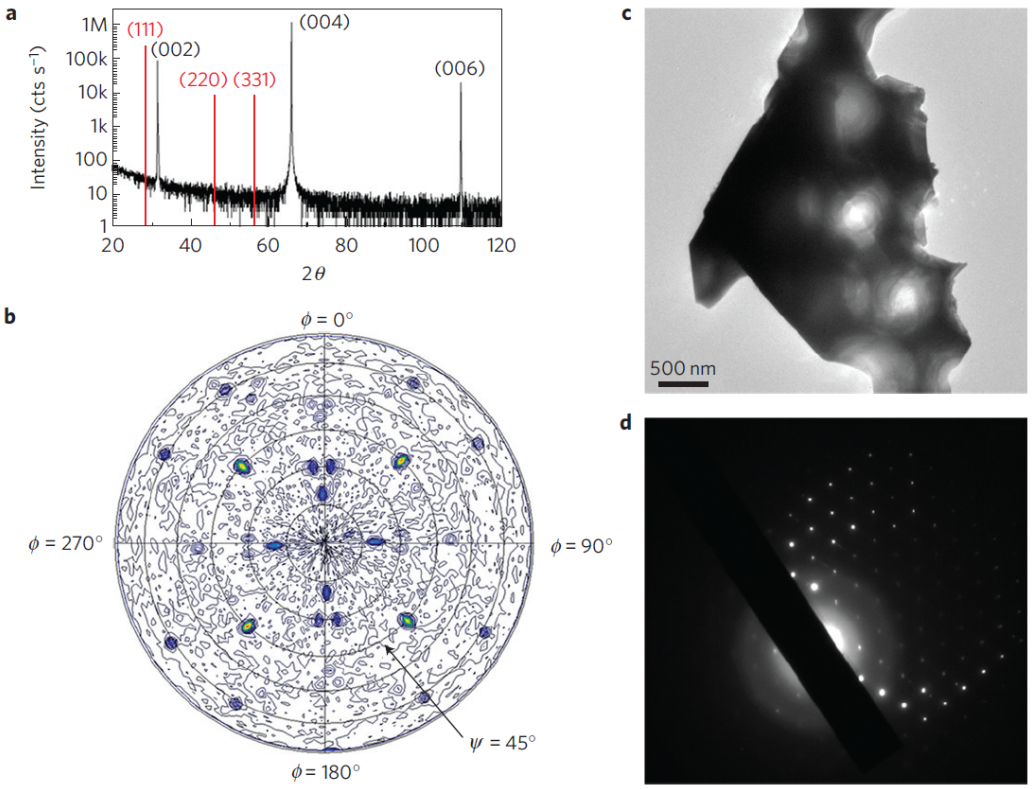


Figure A.2: Verification of epitaxy during 3D patterned growth. (a) $2\theta/\omega$ X-ray diffraction measurement of a GaAs 3D photonic crystal. The red lines and labels are the expected locations for polycrystalline reflection peaks, which are not observed. (b) Pole figure (220) X-ray diffraction measurement of the same photonic crystal. The individual peaks from the (220) family of planes are observed at $\psi = 45°$, rather than a circumferential ring of intensity, as are peaks due to (111) twinning. The scale rings are in 15° increments. (c) Transmission electron micrograph of a small piece of a GaAs photonic crystal grown by 3D SAE. (d) Electron diffraction from the structure in (c).

proaching zero as the number of layers of the template decreases from 11 to 9 to 6. Finite element modeling of the Group III source concentration profile over the 3D mask was used to calculate the partial pressure threshold for heterogeneous nucleation [108, 107]. Diffusion through the 3D mask was modeled using Knudsen and Enskog diffusion [109], allowing calculation of the partial pressure above the mask for the structures with 11, 9 and 6 layers (Figure A.3(f), red circles). The threshold partial pressure for nucleation on the surface of this template is defined to be approximately the partial pressure over the six-layer mask (Figure A.3(e)), as nucleation did not occur in this region. The reactor pressure and inlet precursor pressures are chosen such that the calculated Group III partial pressure over even the thickest region is maintained well below the nucleation threshold (Figure A.3(f), black circles), resulting in nucleation-free growth (for example Figure A.1(a)).

Epitaxial growth alone is not sufficient for optoelectronic device operation. Surface recombination is a significant concern in Group III-V optoelectronic devices, and the porous material shown in Figure A.1(c) has a large surface area. Unoccupied bonds at surfaces act as carrier traps, resulting in non-radiative recombination and significant decreases in device efficiency. This can be prevented by growth of a wider bandgap semiconductor passivation layer on exposed surfaces, creating a potential barrier that prevents carriers from reaching unoccupied bonds. We demonstrate that this may be achieved on a non-planar, 3D material architecture by growing a GaAs/AlGaAs/GaAs heterostructure on all exposed surfaces of the 3D structure after removal of the template (Figure A.4(c), a monolayer to highlight the faceting). The approximately 10 nm $Al_{0.75}Ga_{0.25}As$ layer has a larger electronic bandgap than InGaAs or GaAs, creating an effective potential barrier for carriers in the structure, whereas the outermost GaAs layer serves to prevent oxidation of the AlGaAs. GaAs growth through the template is defined by the template geometry; however, after removal of the template, the AlGaAs growth will occur at different rates for different crystallographic directions. The smooth curvature of the template (Figure A.3(b)) thus gives way to the faceted structure seen in Figure A.3(c), as certain planes grow faster than others, indicating epitaxial growth of the passivation layer on the underlying structure. The effectiveness of the passivation process is characterized by the intensity of the photoluminescence signal before and after passivation, which is related to the relative amount of surface recombination. Photoluminescence

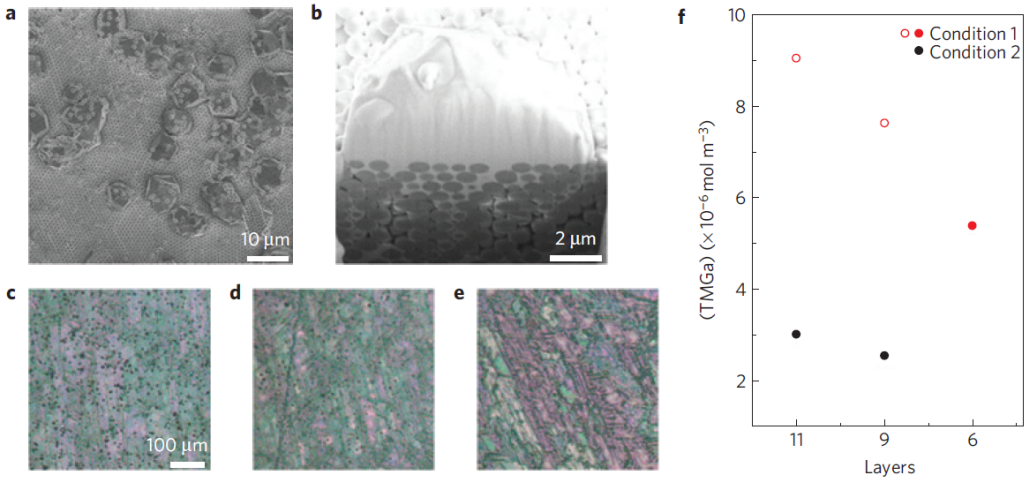


Figure A.3: Heterogeneous nucleation behaviour during 3D selective area epitaxy. (a) Top surface of a 3D template after growth of GaAs under conditions that yield polycrystalline nucleation on the mask. (b) Focused ion-beam cross-section through a polycrystalline nuclei. (c)-(e) Optical micrographs of 3D template surface from regions of 11, 9 and 6 layers, respectively, with varying degrees of polycrystalline nucleation (black spots). (f) Plot of partial pressure of monomethylgallium over the 3D mask surface as a function of template thickness (number of layers), calculated by finite-element modeling. Red circles are under the conditions used to grow the samples shown in (c)-(e) and black circles are after a reduction of the inlet flow rate of the Group III source, as described in the text. Open circles denote conditions where nucleation occurs and closed circles denote nucleation-free growth.

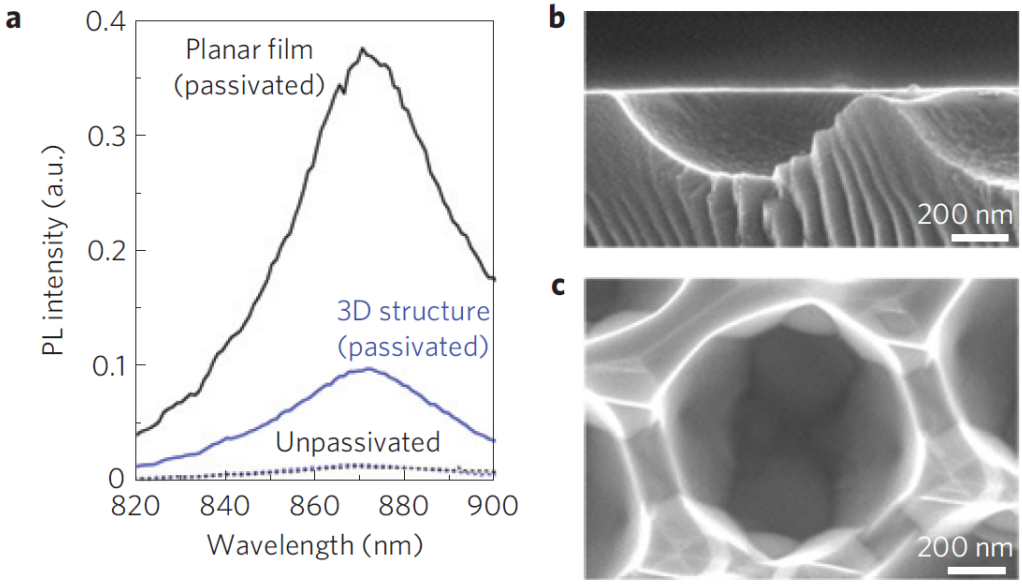


Figure A.4: Surface passivation of 3D structured Group IIIV materials. (a) Photoluminescence measurements of a 3D structured (blue) and unpatterned (black) material before (dashed) and after (solid) passivation. Before passivation, the photoluminescence of both samples is low and essentially overlaps. (b) GaAs structure after inversion grown partially through the first layer of a template. The curvature imparted by the template is clearly visible. (c) The structure from (b) after growth of a passivation layer (GaAs/AlGaAs/GaAs). The epitaxial nature of the passivation layer is highlighted by the faceting of the structure.

(PL) from a multilayer 3D structure and planar, unpatterned film grown concurrently on the same substrate exhibit similar PL before passivation and an increase in PL intensity of about an order of magnitude or more after (Figure A.4(a)). The unpatterned material exhibits approximately three times greater PL signal than the 3D structure after passivation, which is probably due to the greater surface area of the 3D structure (by approximate factor of II). By optimization of the passivation process, 3D structures that exhibit a 20 times increase in photoluminescence after passivation have been obtained.

The most important feature of the 3D SAE process is that growth begins at the substrate and extends upwards while preserving epitaxy, enabling formation of chemically and electrically complex heterostructures. The complex 3D photonic crystal optoelectronic devices proposed for many years, but never realized, require epitaxially grown 3D structured semiconductor materials

with electronic dopants and embedded light-emitting (or collecting) heterojunctions. We demonstrate such a device by fabricating a 3D photonic crystal LED using 3D selective area epitaxy. The device was grown by incorporating an InGaAs layer between lower (Si-doped) and upper (C-doped) GaAs cladding layers during growth through the 3D template, thereby defining a light-emitting heterostructure within a 3D PhC (Figure A.5(a)). The final 3D photonic crystal LED (Figure A.5(a),(b)) consists of a 120 μm diameter ring electrode on the top of a 3D PhC cylindrical mesa (the mesa serves to prevent current spreading beyond the device boundary). The light-emitting layer consists of approximately 15 nm InGaAs ($\sim$50% indium), bounded on each side by 800 nm of undoped GaAs and thicker layers of Si and C-doped GaAs. An array of devices show excellent electrical rectification and device-to-device reproducibility. The electrically driven emission from a device is shown in Figure A.5(c)-(e) at increasing drive currents. At 2 mA the mesa is emitting light from the entire device, with the strongest emission from the center of the ring electrode. At higher drive currents the light output increases as expected. Electroluminescence (EL) spectra collected from a device at varying drive currents (Figure A.5(g)) exhibited a peak emission wavelength of 1,230 nm, which was invariant with drive current. The light output increased linearly over the studied current range.

The emission of two devices with different lattice constants was compared to observe the effects of the PhC structure on the behavior of the device. The EL spectra were measured before and after infiltration of a solvent (either dodecane or o-xylene), which is used to change the refractive index contrast of the system. The device with lattice constant a = 735 nm shows no change in spectral shape due to infiltration of the solvent, indicating that the interaction of light with the periodic material is minimal. The only change is an increase in the emission intensity due to reduced scatter from the PhC surface when the refractive index contrast is reduced. Conversely, the device with the larger lattice constant (a = 1,030 nm) demonstrates a noticeable change in peak shape on infiltration of the solvent. This indicates that the emission spectrum of this device is probably modulated by interaction of the InGaAs with the modified optical density of states of the 3D structure. Our band structure calculations suggest this is the case, however we do not draw extensive conclusions, if for no other reason than the fact that the finite thickness of the device leads to a disparity between experiment and band

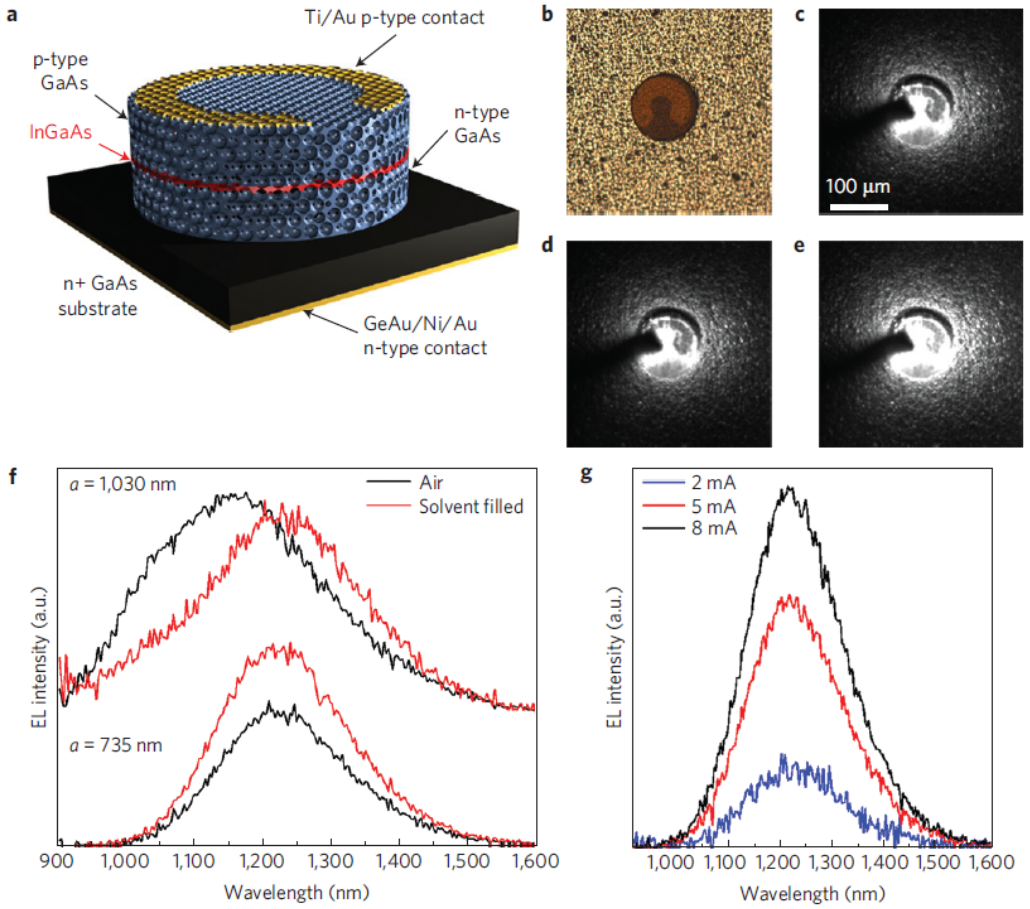


Figure A.5: Electrically driven emission from 3D photonic crystal LED. (a) Schematic of a GaAs 3D photonic crystal (blue) containing an InGaAs light-emitting layer (red). The structure is lithographically patterned into the form of a cylindrical mesa with a ring electrode on the top surface (gold). (b) An optical micrograph of a device under white light illumination showing the Ti/Au ring electrode and the mesa surrounded by the etched GaAs. (c-e) Following current injection ((c), 2 mA, (d), 4 mA, (e), 6mA) light is emitted and collected by an infrared camera. The light output increases with current. (f) Electroluminescence (EL) spectra from 3D photonic crystal (PhC) LEDs with lattice constants of 735 nm and 1,030 nm respectively. The shape of the EL spectrum from the 735 nm lattice constant structure does not change when the pores are filled with dodecane, whereas the EL spectrum from the 1,030 nm lattice constant structure changes significantly when the pores are filled with o-xylene. The EL spectra from the 1,030 nm lattice constant structure are shifted up for clarity. (g) EL spectra from a 3D PhC LED where the emission is not modified by the 3D structure (a = 735 nm). The EL intensity increases linearly with current.

structure calculations.

We have developed a novel 3D SAE approach to create optoelectronically active 3D nanostructured Group III-V semiconductor devices. We highlight this approach as a unique route to 3D nanostructured optoelectronic devices by fabricating, and demonstrating electrically driven emission from, a 3D photonic crystal LED, which has not been achieved by other means. The improvements in device performance that will lead to the future application of 3D architectured materials in practical injection electroluminescent devices will require significant efforts to concurrently maximize both optical and electronic properties. Research will need to address, for example, the photonic band structure, electrical conductivity and surface passivation. The end result will be a powerful new optoelectronic device technology with wide applicability.

A.3 Methods

A.3.1 Template fabrication

Colloids were synthesized using the methods of Stöber et al. [110] and colloidal crystal templates were formed using methods similar to previously published techniques [111]. Sphere diameters used in this work were 520, 760 and 920 nm, which were calcined for 13 h at 720 °C (520 and 760 nm) and 72 h at 600 °C (920 nm). Templates formed using multibeam interference lithography were fabricated in SU-8 photoresist (MicroChem, SU-8 2000 series) using a 532nm frequency-doubled Nd:YVO_4 laser according to previously published procedures [112, 113]. The SU-8 was spin-coated on GaAs substrates that had an e-beam evaporated TiO_2 antireflection coating. Photoresist templates were converted to aluminum oxide using a Cambridge Nanotech ALD system. The photoresist and TiO_2 were removed using a high-pressure (500 mtorr) reactive ion etch (20 sccm O_2, 2 sccm CF_4) at 150 W (the TiO_2 underneath the alumina was not undercut, allowing the alumina template to remain on the TiO_2-coated GaAs substrate). Silica template removal was achieved using a buffered oxide etch (Transene, Buffered-HF Improved). Alumina templates were removed using a mixture of 10% HF, 45% water and 45% ethanol.

A.3.2 MOCVD growth and device fabrication

MOCVD growth was performed in an Aixtron 200/4 low-pressure MOCVD reactor at 50 mbar. Arsine was used as the Group V source and trimethylgallium, trimethylindium and trimethylaluminium were used as Group III sources. Growth temperatures ranged from 625 to 800 °C depending on alloy composition and dopant gas used. Samples were doped using disilane (silicon, n type) and carbon tetrabromide (carbon, p type). All substrates were epi-ready GaAs from AXT Technologies (GaAs:Si, 1-3$\times 10^{18}$ cm^{-3}). Typical precursor flow rates were 15,000 sccm H_2, 5×10^{-4} mol m^{-1} arsine, 10^{-5} mol m^{-1} trimethylgallium and 10^{-6} mol m^{-1} trimethylindium. The growth rate varies significantly with PhC lattice constant, fill factor and number of layers. The range of growth rates used for this work was 0.04-0.5 nm s^{-1}. Contacts were evaporated onto the samples using a CHA SEC-600 electron-beam/thermal evaporator. The contact materials are Ge/Au/Ni/Au for n-type contacts and Ti/Pt/Au for p-type contacts (n-type contacts were alloyed at 350 °C for 120 s under hydrogen).

Before MOCVD growth, samples were degreased using a 5 m acetone rinse (twice), 2 m methanol rinse, 2 m isopropylalcohol rinse and then blown dry. Samples were then cleaned in an O_2 plasma (TI Planar Plasma etch) at 300 W for 10 m. Before loading into the reactor an oxide etch was performed using 50:50 HCl:H_2O. Each growth step, apart from AlGaAs capping, was preceded with a 10 m oxide bakeout at 750 °C. For AlGaAs passivation growth processes a 1:10 ammonia:water oxide etch was performed in a glovebox connected to the MOCVD reactor to prevent oxidation of the sample before loading into the reactor; no oxide bakeout was performed.

Devices were fabricated by first depositing n-type contacts on the back surface of each sample and annealing. The ring contact was deposited using a custom-made kapton shadow mask. The samples were then coated with 900 nm of SiO_2 using plasma-enhanced chemical vapor deposition (PECVD) and coated with photoresist (AZ4620). The photoresist was patterned to leave a circle over the ring electrodes and the exposed SiO_2 was subsequently etched using reactive-ion etching (RIE; CF_4;O_2). Samples were dipped in buffered HF (Transene, Buffered HF Improved) for 30 s, rinsed in isopropylalcohol and dried under nitrogen. A 60 s O_2 plasma clean of the samples was performed, followed by inductively coupled plasma-RIE (ICP-RIE) etching of the GaAs

($SiCl_4$, Ar) to form a mesa. The remaining SiO_2 was then removed with a 5 m dip in buffered HF.

A.3.3 Device characterization

Scanning electron micrographs were taken on a Hitachi S-4800 SEM or FEI Dual Beam 235 focused ion-beam lithography system. X-ray diffraction measurements were performed on a Phillips X'Pert MRD system with a 4-bounce germanium monochromator and PIXcel line detector. Photoluminescence measurements were taken using an Ar-ion laser operating at 488 nm and either an InGaAs detector with a lock-in amplifier or Princeton Instruments Si CCD detector. Electroluminescent samples were measured using a Control Development fibre-coupled InGaAs CCD detector with single-stage thermoelectric cooling. Infrared micrographs were taken using a XenICs Xeva-FPA-1.7-320 attached to a Bruker Hyperion microscope with a 10× glass objective (NA = 0.1).

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